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# MS-7758

## Intel -MahoBay plamform H77

ATX

Ver: 10(304.8x243.84)

CPU:

IVY bridge LGA1155

System Chipset:

Panther Point H77(CO-LAY Z77)

Onboard Chip:

HD Audio Codec:ALC892 colay 887

LAN-RTL8111E colay8105E

SIO:Fintek F71868AD

Flash ROM: SPI 64 MB

Main Memory:

DDRIII (1066/1333/1600MHz) \* 4 (Dual Channel)

ACPI:

UPI

PWM:

VRD12 -UT501 3+1 Phase

Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1 ) Slot \* 2

PCI Express (X4 ) Slot \* 1

PCI Slot \* 3

Other:

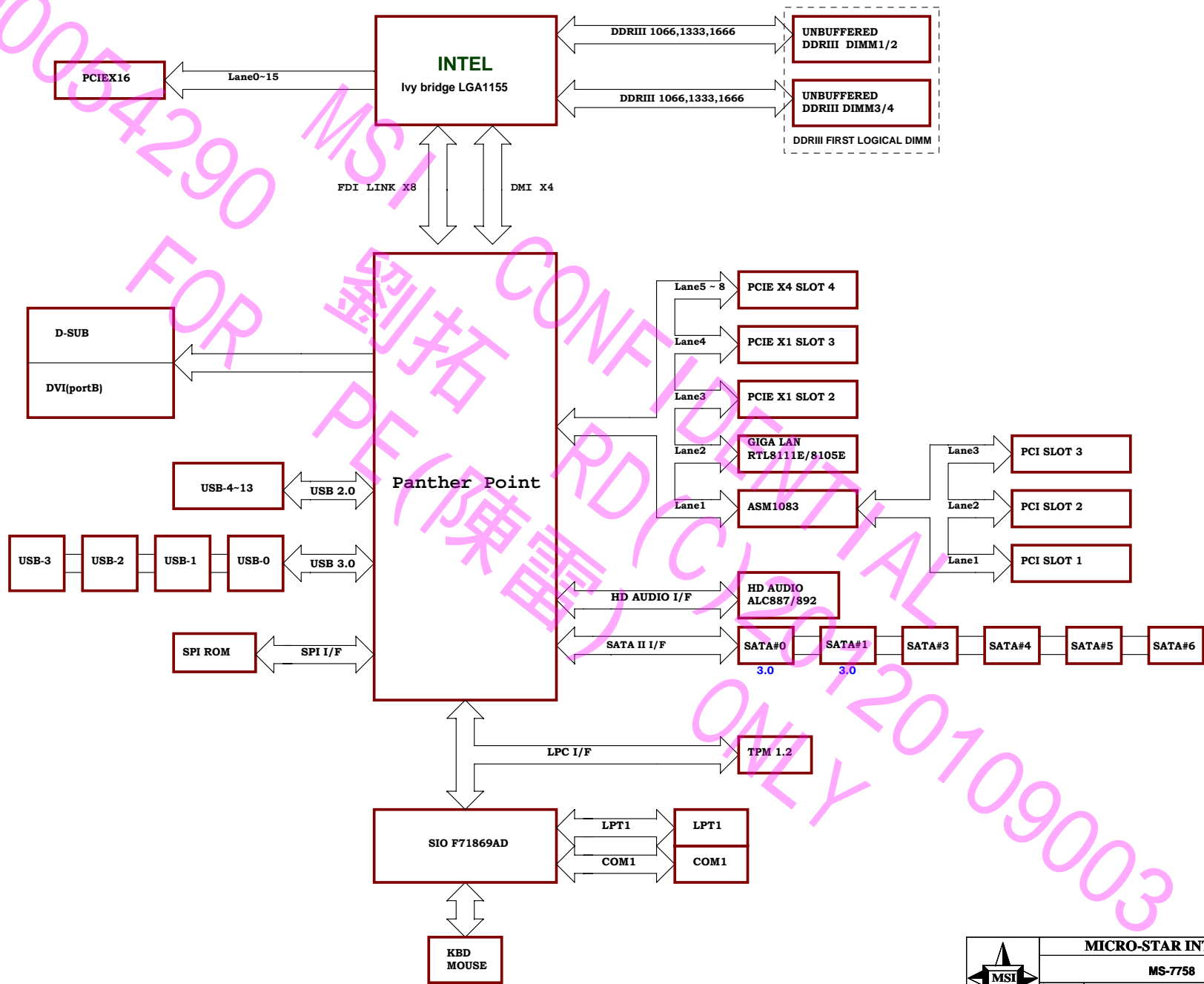
SATA3.0 x2+SATA2.0 x4 (PCH)

USB2.0 \*10

REAL USB3.0 \*2

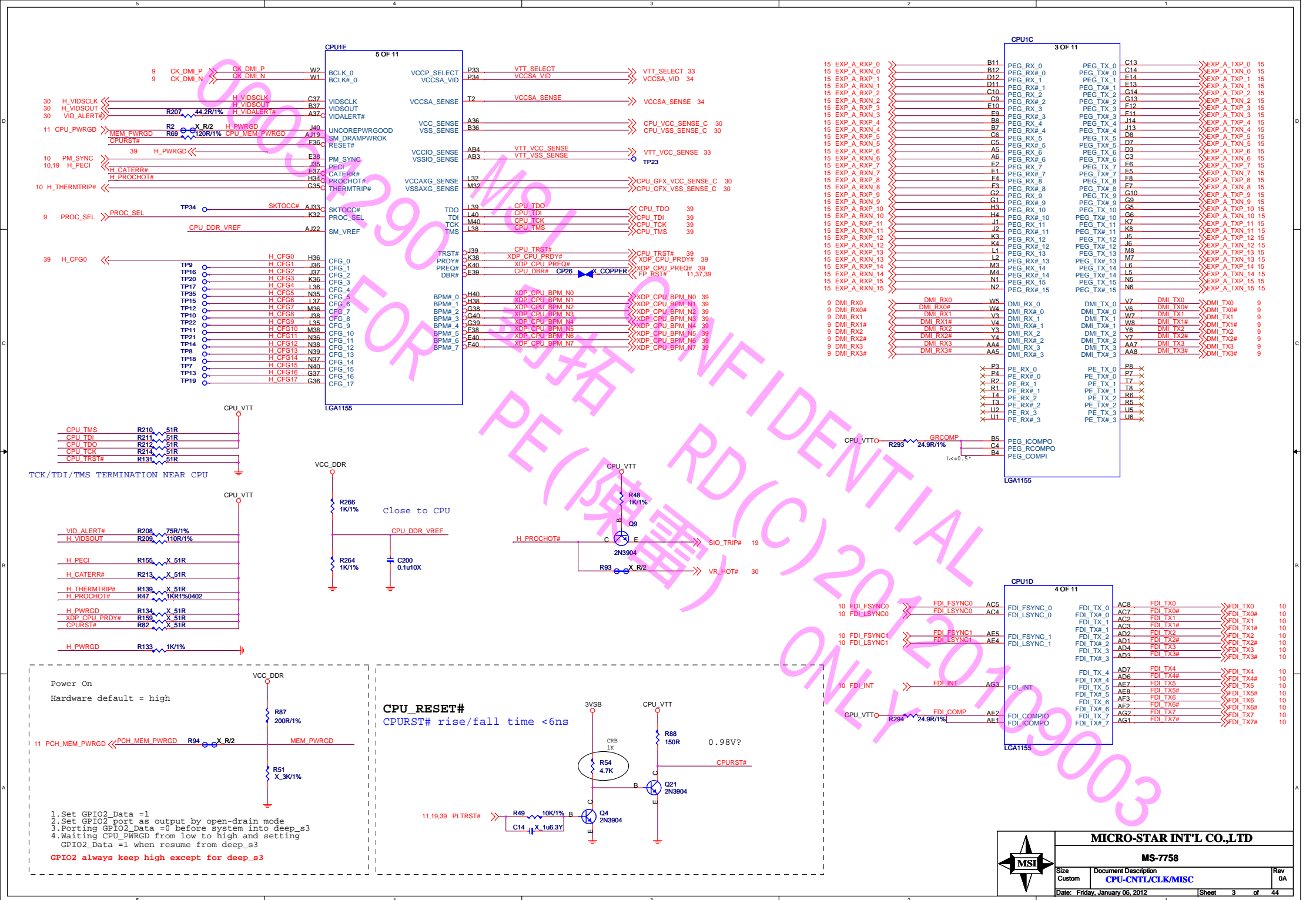
FRONT USB3.0 \*2

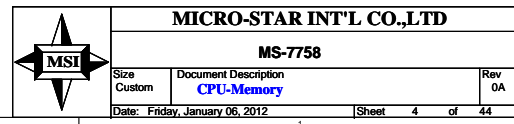
MS-7758 Block Diagram

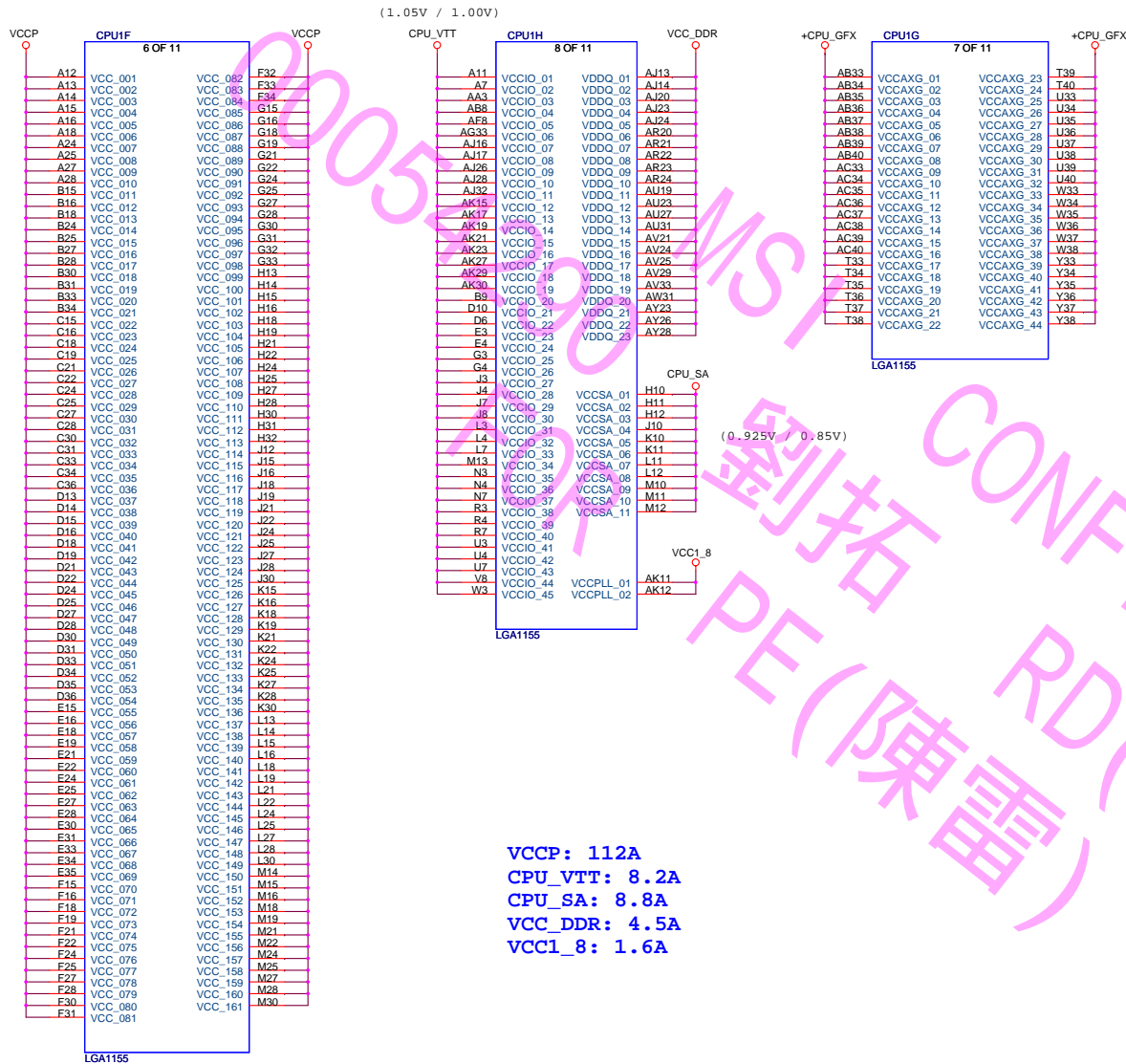


Slot Sequence:

- PCIE X1
- PCIE X16
- PCIE X1
- PCI SLOT
- PCIE X16(X4)
- PCI SLOT
- PCI SLOT

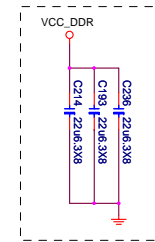






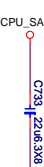
### +1.5V\_DDR3-Decoupling

CPU SOCKET CAVITY CAPS



### +CPU\_SA Decoupling

Backside



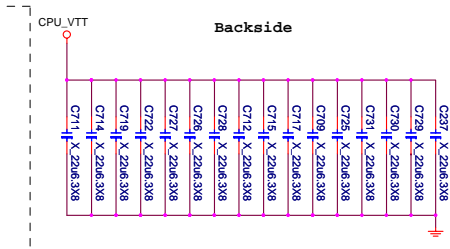
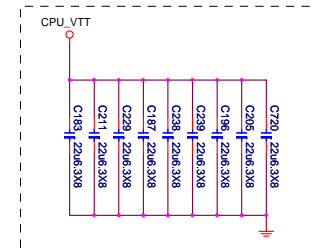
### +VCC1\_8 Decoupling

Backside



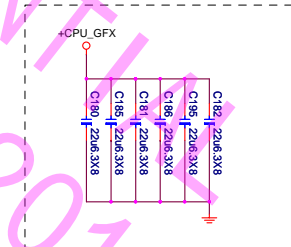
### +CPU\_VTT Decoupling

CPU SOCKET CAVITY CAPS

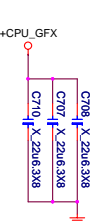


### +CPU GFX Decoupling

CPU SOCKET CAVITY CAPS



Backside

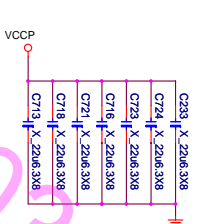


### +CPU VCCP-Decoupling

CPU SOCKET CAVITY CAPS



Backside



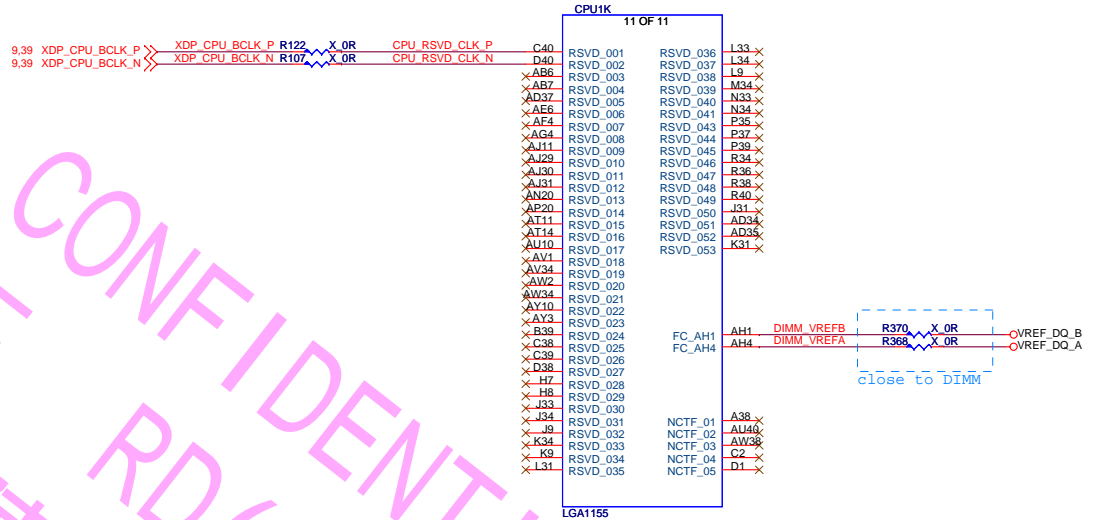
MICRO-STAR INT'L CO.,LTD

MS-7758

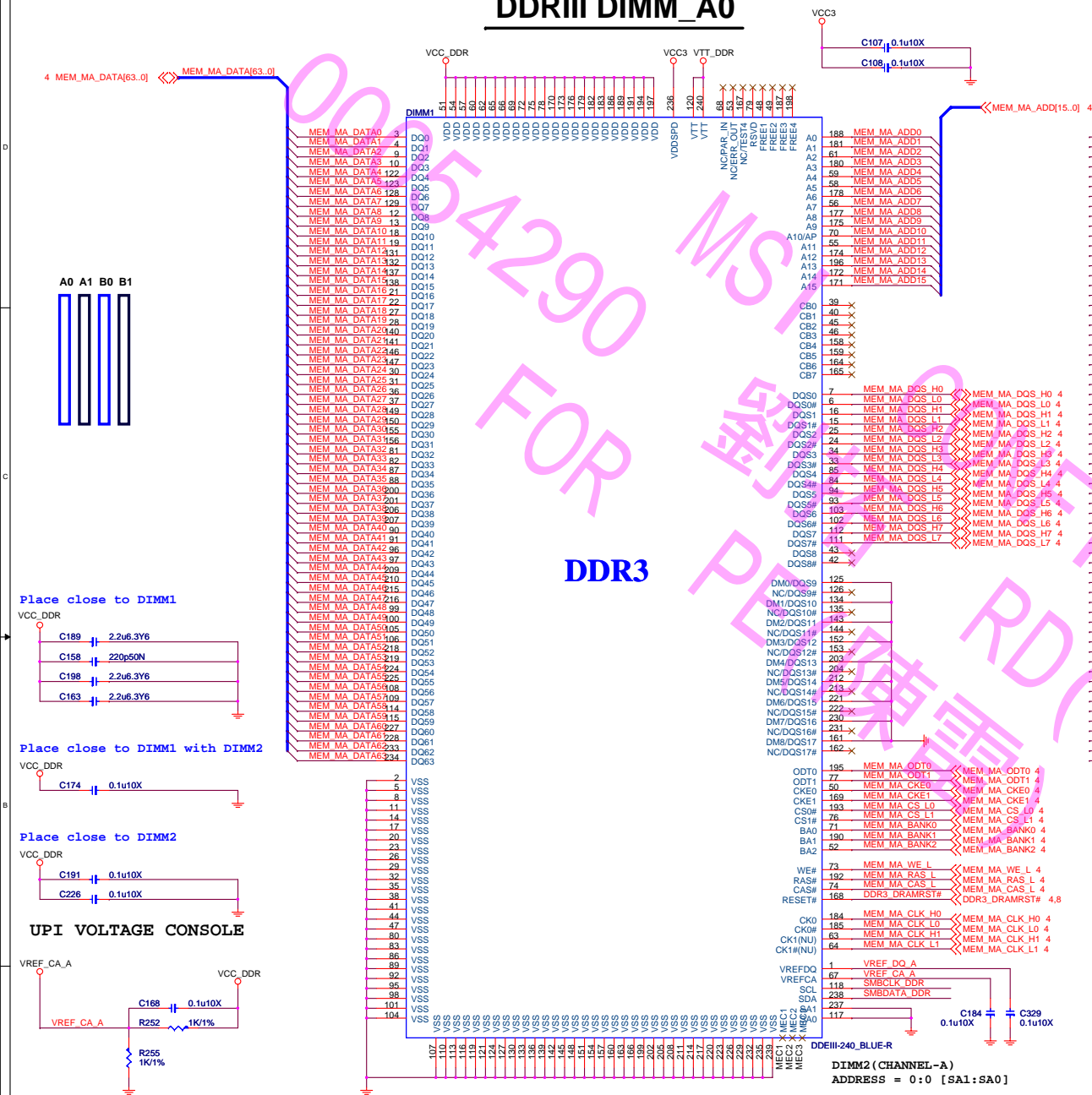
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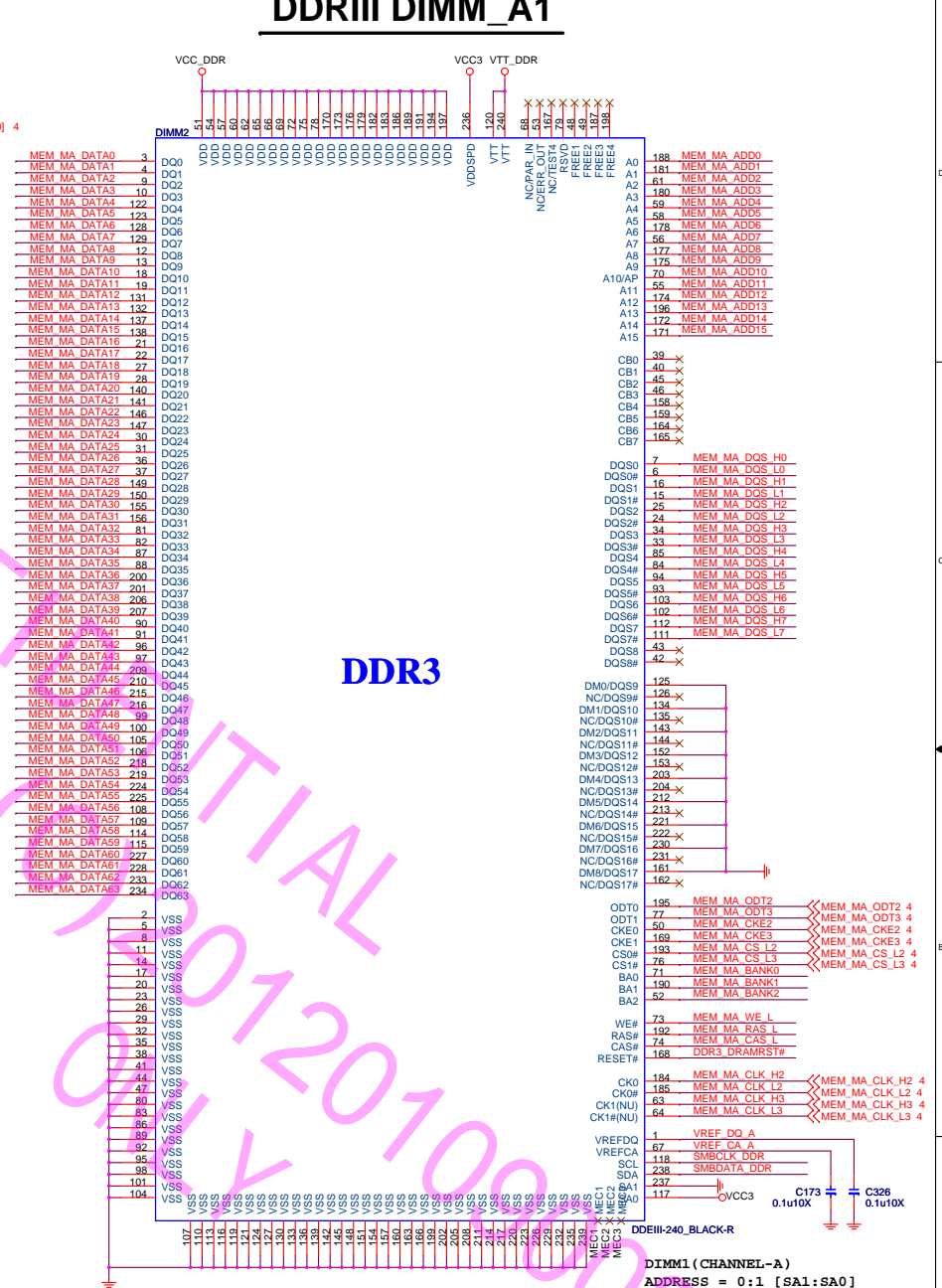
CPU1J			CPU1J		
9 OF 11			10 OF 11		
A17	VSS_001	AM27	AV11	VSS_181	H37
A23	VSS_002	AM3	AV14	VSS_182	H39
A26	VSS_003	AM30	AV17	VSS_183	H5
A29	VSS_004	AM36	AV3	VSS_184	H6
A35	VSS_005	AM37	AV35	VSS_185	H6
AA33	VSS_006	AM38	AV38	VSS_186	H11
AA34	VSS_007	AM39	AV6	VSS_187	J17
AA35	VSS_008	AM4	AW10	VSS_188	J20
AA36	VSS_009	AM40	AW11	VSS_189	J23
AA37	VSS_010	AM44	AW14	VSS_190	J26
AA38	VSS_011	AN10	AW16	VSS_191	J29
AA6	VSS_012	AN11	AW36	VSS_192	J32
AB5	VSS_013	AN14	AW6	VSS_193	K1
AC1	VSS_014	AN17	AY11	VSS_194	K12
AC6	VSS_015	AN19	AY14	VSS_195	K13
AD33	VSS_016	AN22	AY18	VSS_196	K14
AD36	VSS_017	AN24	AY35	VSS_197	K17
AD38	VSS_018	AN27	AY4	VSS_198	K2
AD39	VSS_019	AN31	AY6	VSS_199	K20
AD40	VSS_020	AN33	AY8	VSS_200	K23
AD5	VSS_021	AN32	B10	VSS_201	K26
AD6	VSS_022	AN33	B13	VSS_202	K29
AE3	VSS_023	AN34	B14	VSS_203	K33
AE33	VSS_024	AN35	B17	VSS_204	K35
AE36	VSS_025	AN36	B23	VSS_205	K37
AF1	VSS_026	AN5	B26	VSS_206	K39
AF34	VSS_027	AN6	B29	VSS_207	K5
AF36	VSS_028	AN7	B32	VSS_208	K6
AF37	VSS_029	AN8	B35	VSS_209	L10
AF40	VSS_030	AN9	B38	VSS_210	L17
AF5	VSS_031	AP1	B6	VSS_211	L20
AF6	VSS_032	AP12	C11	VSS_212	L23
AF7	VSS_033	AP14	C12	VSS_213	L26
AG36	VSS_034	AP17	C17	VSS_214	L29
AH2	VSS_035	AP22	C20	VSS_215	L8
AH3	VSS_036	AP25	C23	VSS_216	L8
AH33	VSS_037	AP27	C26	VSS_217	M17
AH36	VSS_038	AP30	C29	VSS_218	M2
AH37	VSS_039	AP36	C32	VSS_219	M20
AH38	VSS_040	AP37	C35	VSS_220	M23
AH39	VSS_041	AP40	C7	VSS_221	M26
AH40	VSS_042	AP5	C8	VSS_222	M29
AH5	VSS_043	AP11	D17	VSS_223	M33
AH8	VSS_044	AP14	D2	VSS_224	M35
AJ12	VSS_045	AP15	D20	VSS_225	M37
AJ15	VSS_046	AP18	D23	VSS_226	M39
AJ18	VSS_047	AP19	D26	VSS_227	M5
AJ21	VSS_048	AP22	D29	VSS_228	M6
AJ25	VSS_049	AP27	D32	VSS_229	M9
AJ27	VSS_050	AP30	D37	VSS_230	M9
AJ36	VSS_051	AP36	D39	VSS_231	P1
AJ5	VSS_052	AR5	D4	VSS_232	P2
AK1	VSS_053	AT1	D5	VSS_233	P36
AK10	VSS_054	AT10	D9	VSS_234	P40
AK13	VSS_055	AT11	E12	VSS_235	P5
AK14	VSS_056	AT13	E15	VSS_236	P6
AK16	VSS_057	AT15	E17	VSS_237	R33
AK22	VSS_058	AT16	E20	VSS_238	R35
AK28	VSS_059	AT17	E23	VSS_239	R37
AK31	VSS_060	AT2	E26	VSS_240	R39
AK32	VSS_061	AT25	E29	VSS_241	R8
AK33	VSS_062	AT27	E32	VSS_242	T1
AK34	VSS_063	AT28	E36	VSS_243	T5
AK35	VSS_064	AT29	E7	VSS_244	T6
AK36	VSS_065	AT3	E8	VSS_245	U8
AK37	VSS_066	AT30	F1	VSS_246	V1
AK4	VSS_067	AT31	F10	VSS_247	V33
AK40	VSS_068	AT32	F13	VSS_248	V34
AK5	VSS_069	AT33	F14	VSS_249	V35
AK6	VSS_070	AT34	F17	VSS_250	V36
AK7	VSS_071	AT35	F2	VSS_251	V37
AK9	VSS_072	AT37	F20	VSS_252	V38
AL11	VSS_073	AT38	F23	VSS_253	V39
AL14	VSS_074	AT39	F26	VSS_254	V40
AL17	VSS_075	AT40	F29	VSS_255	V5
AL19	VSS_076	AT4	F35	VSS_256	W6
AL24	VSS_077	AT5	F37	VSS_257	Y5
AL27	VSS_078	AT6	F39	VSS_258	Y8
AL30	VSS_079	AT7	F5	VSS_259	
AL36	VSS_080	AT9	F6	VSS_260	
AL5	VSS_081	AT9	F9	VSS_261	
AM1	VSS_082	AT9	G11	VSS_262	
AM11	VSS_083	AT9	G12	VSS_263	
AM14	VSS_084	AT9	G17	VSS_264	
AM17	VSS_085	AT9	G20	VSS_265	
AM2	VSS_086	AT9	G23	VSS_266	
AM21	VSS_087	AT9	G26	VSS_267	
AM23	VSS_088	AT9	G29	VSS_268	
AM25	VSS_089	AT9	G34	VSS_269	
	VSS_090	AT9	G7	VSS_270	
			G8	VSS_271	
			H1	VSS_272	
			H17	VSS_273	
			H2	VSS_274	
			H20	VSS_275	
			H23	VSS_276	
			H26	VSS_277	
			H29	VSS_278	
			H33	VSS_279	
			H35	VSS_280	



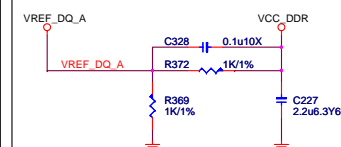
## DDRIII DIMM\_A0



## DDRIII DIMM\_A1



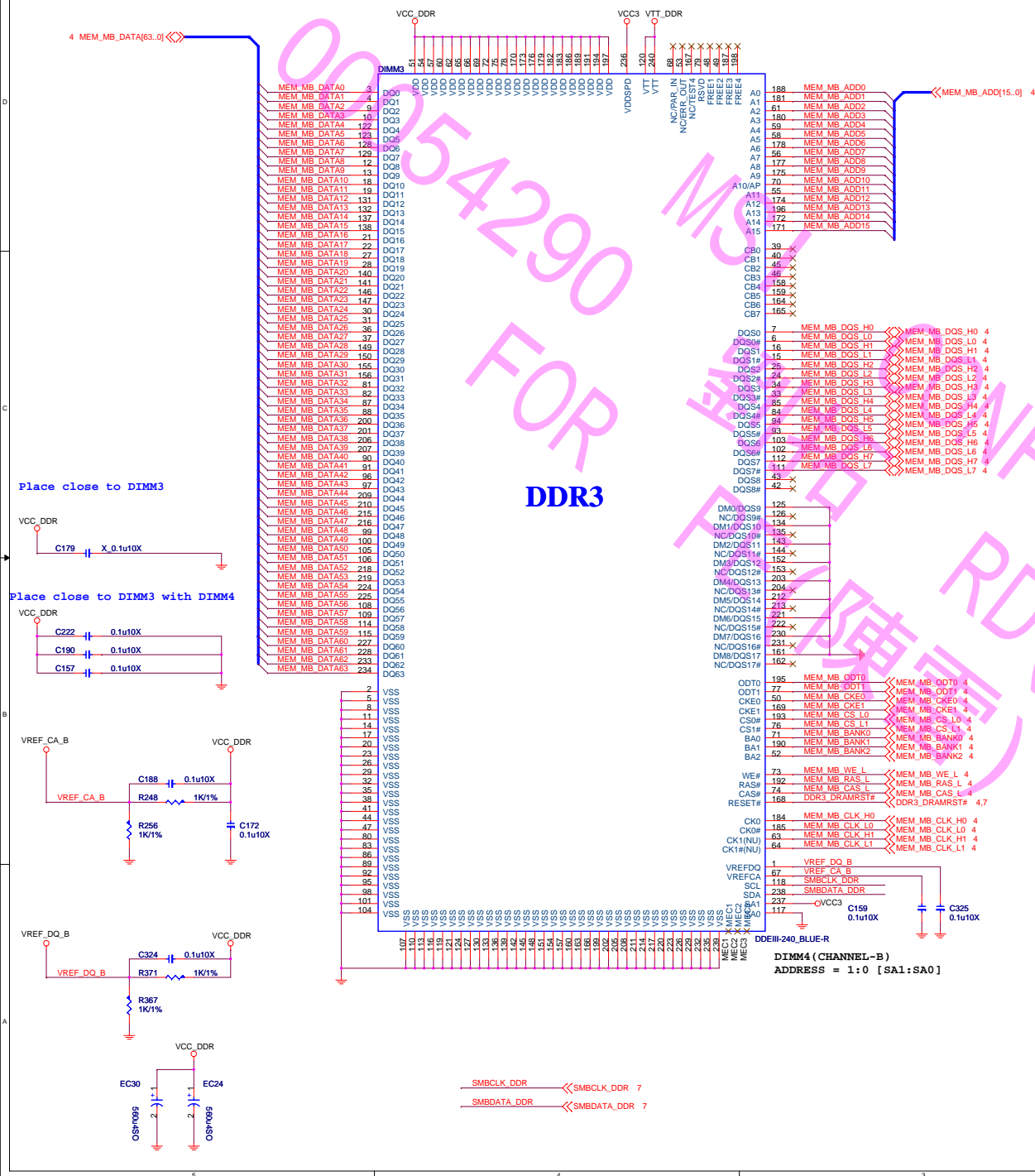
## UPI VOLTAGE CONSOLE



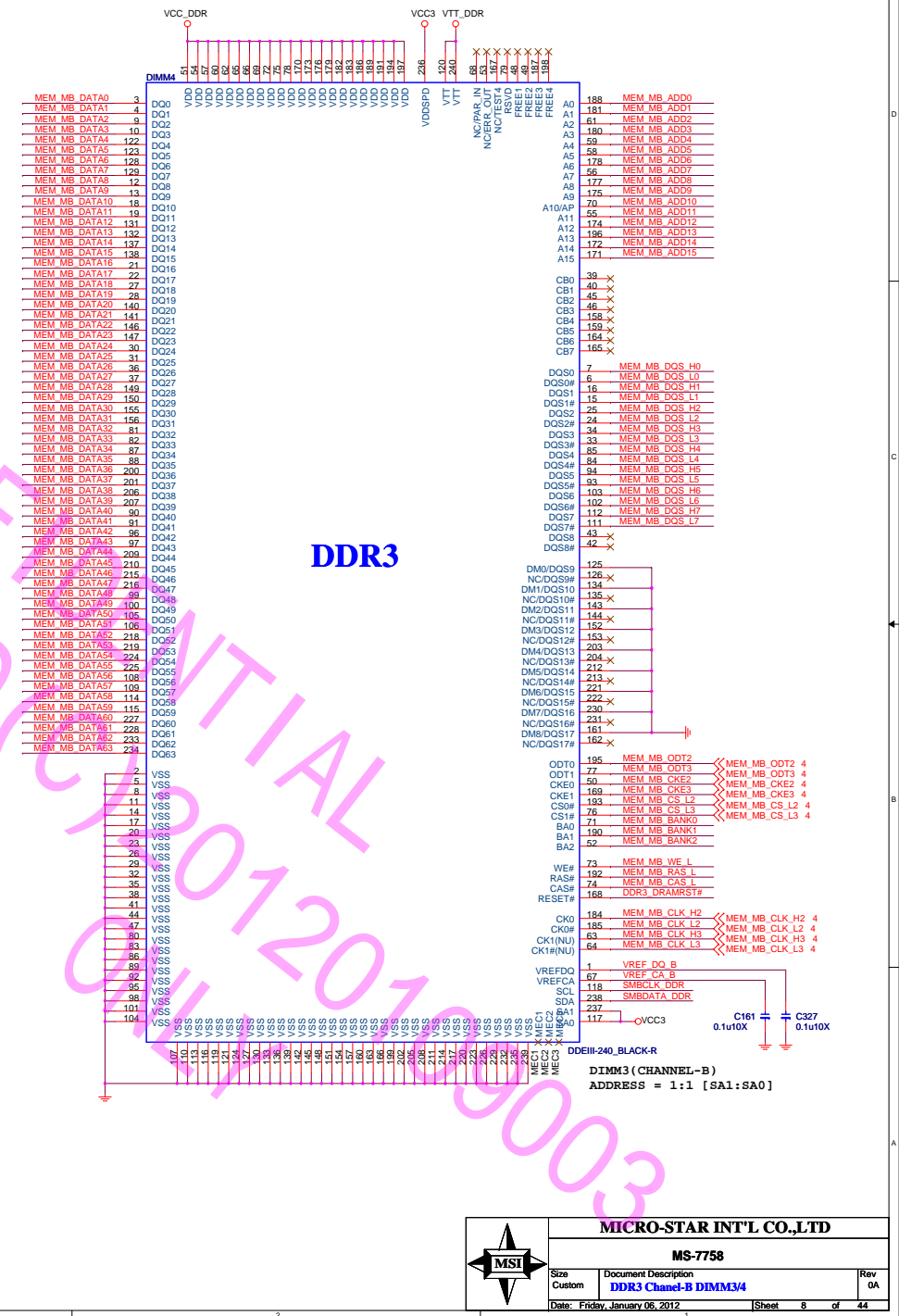
8 SMBCLK\_DDR >> SMBCLK\_DDR R180 33R << SMBCLK 11,15,16,30,37,39

8 SMBDATA\_DDR >> SMBDATA\_DDR R187 33R << SMBDATA 11,15,16,30,37,39

## DDRIII DIMM\_B0



## DDRIII DIMM\_B1

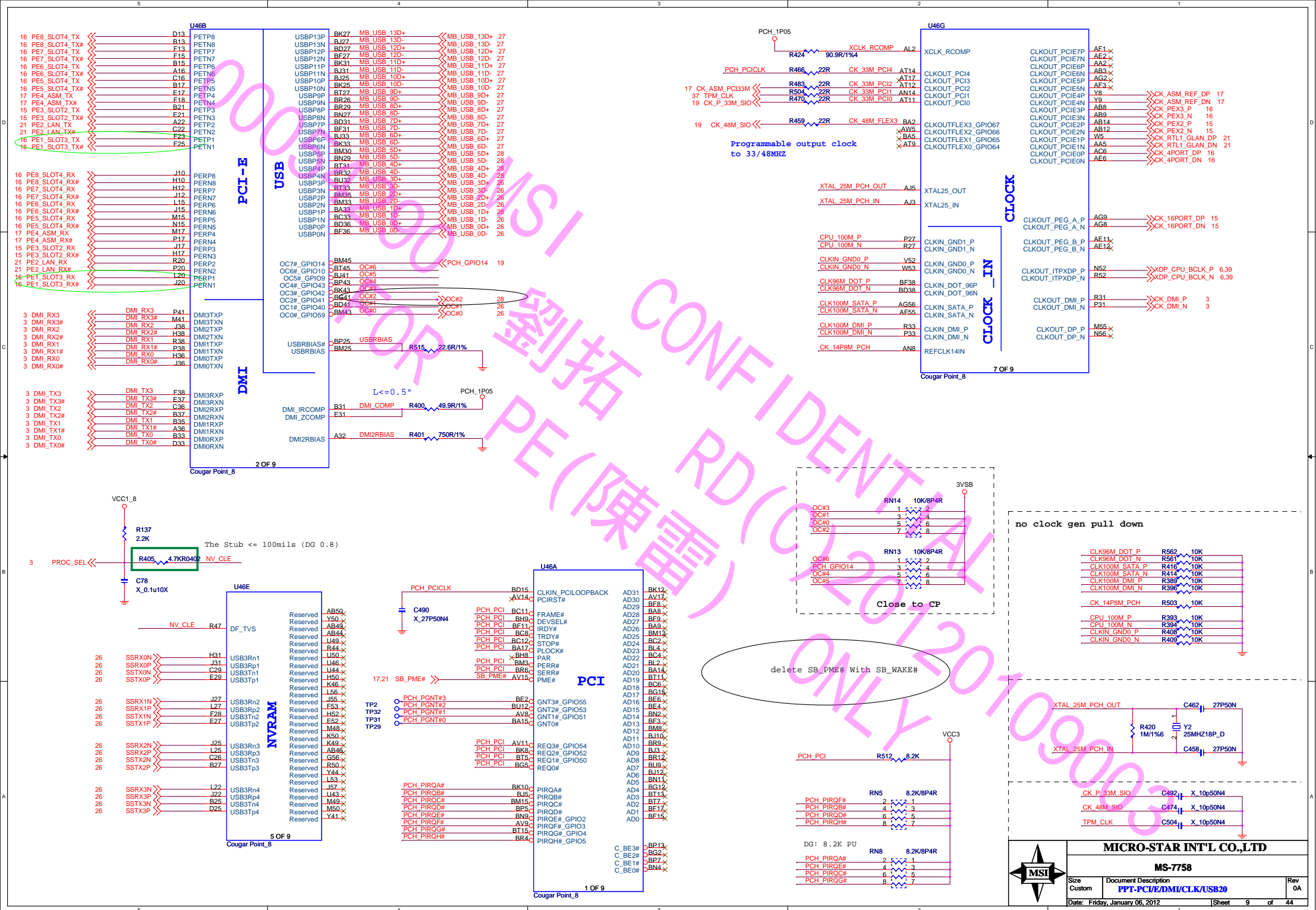


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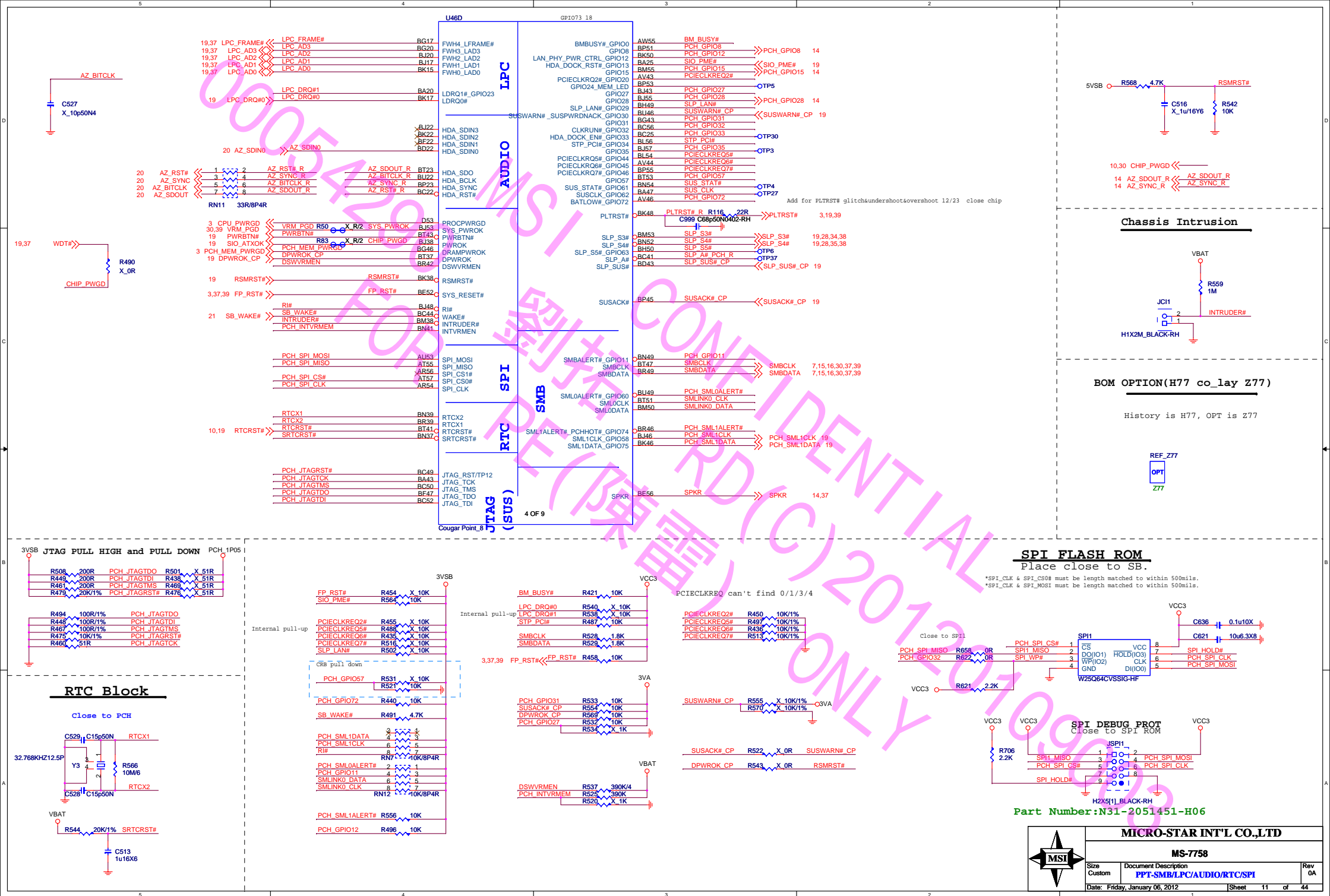
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Size Custom	Document Description <b>DDR3 Chanel-B DIMM3/4</b>	Rev 0A
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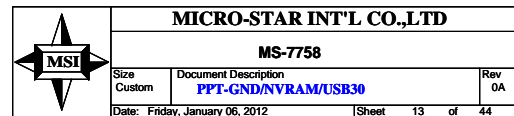






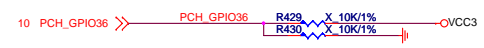
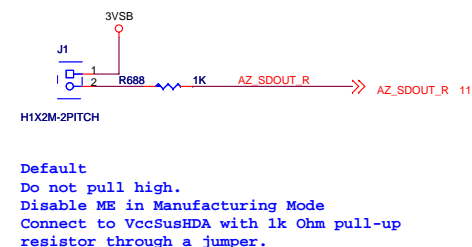
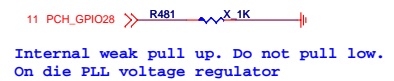
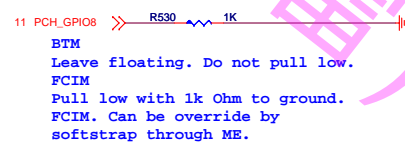
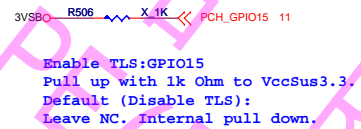
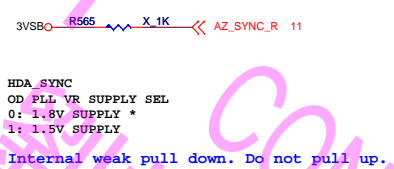
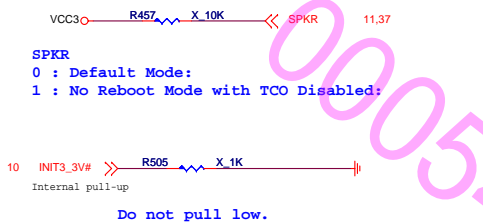








PCH Straps

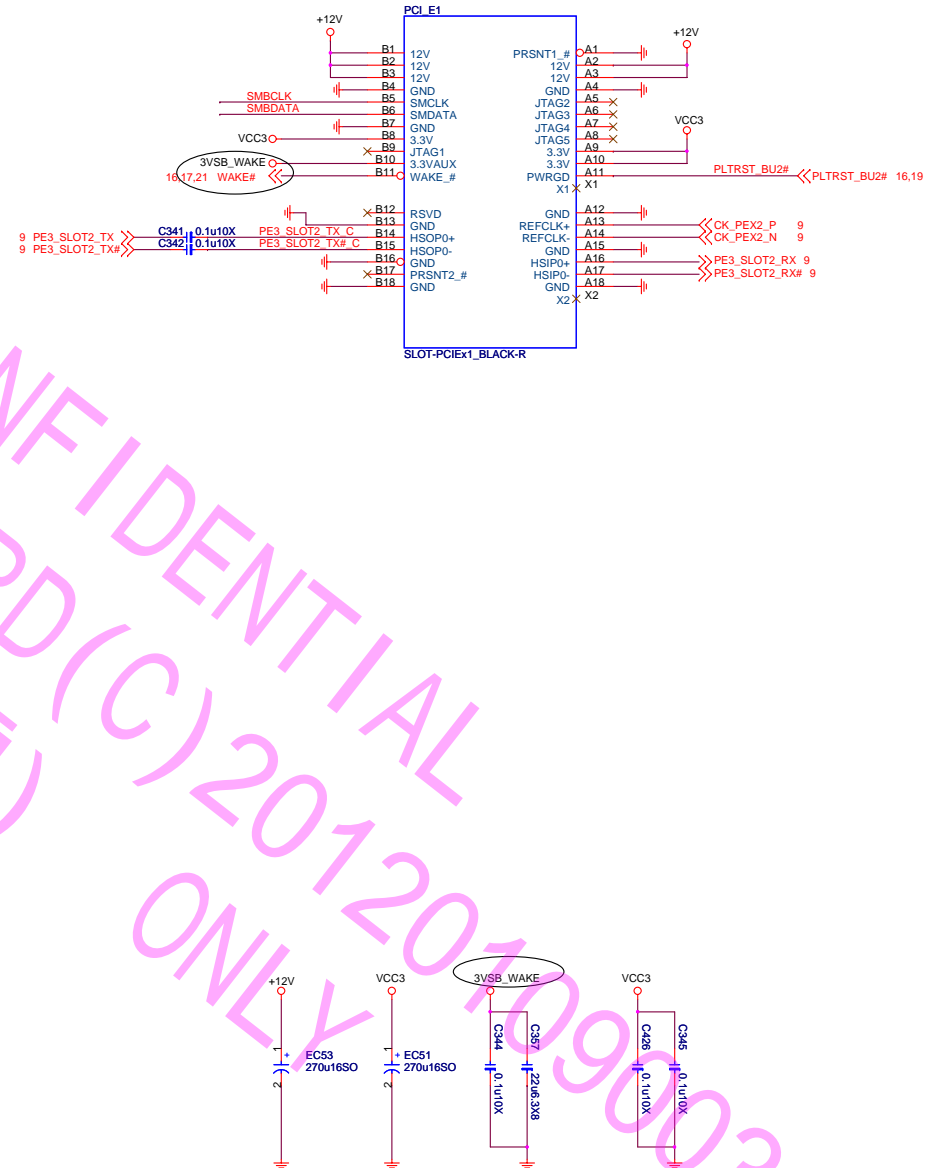


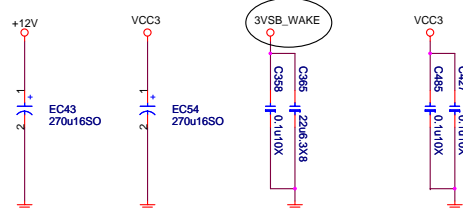
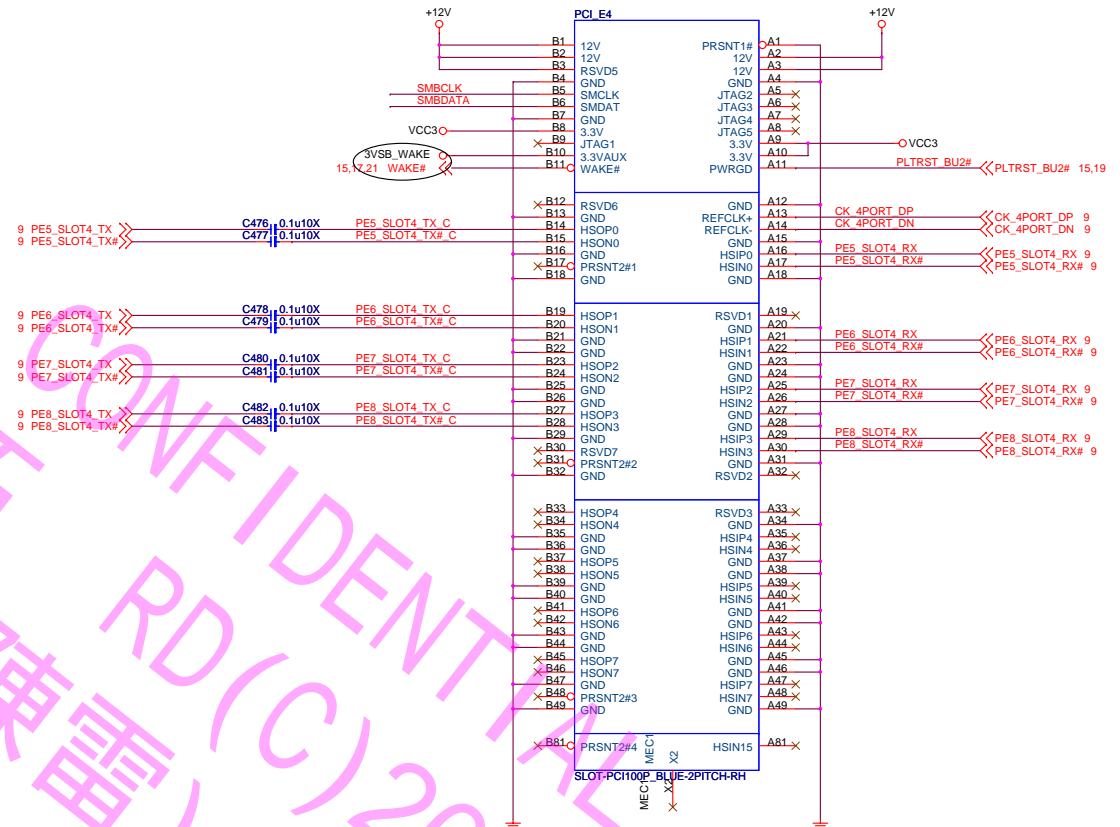
Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:  
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3\_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.  
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window  
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.



Since Pin has strap functionality that requires internal pull-down to be sampled at rising PWROK, following guidelines are required to be followed:  
a) When Used as SATA2GP/SATA3GP for Mechanical Presence detect - Use a weak external pull-up (150K-200K ohms) to Vcc3\_3 OR use 10K external pull-up that is enabled only after PLTRST# de-assertion.  
b) When Used as GP Input (Pin HW default) Ensure GPI is not driven high during strap sampling window  
When Unused as GPIO or SATA[x]GP Use 8.2K-10K pull-down to ground.

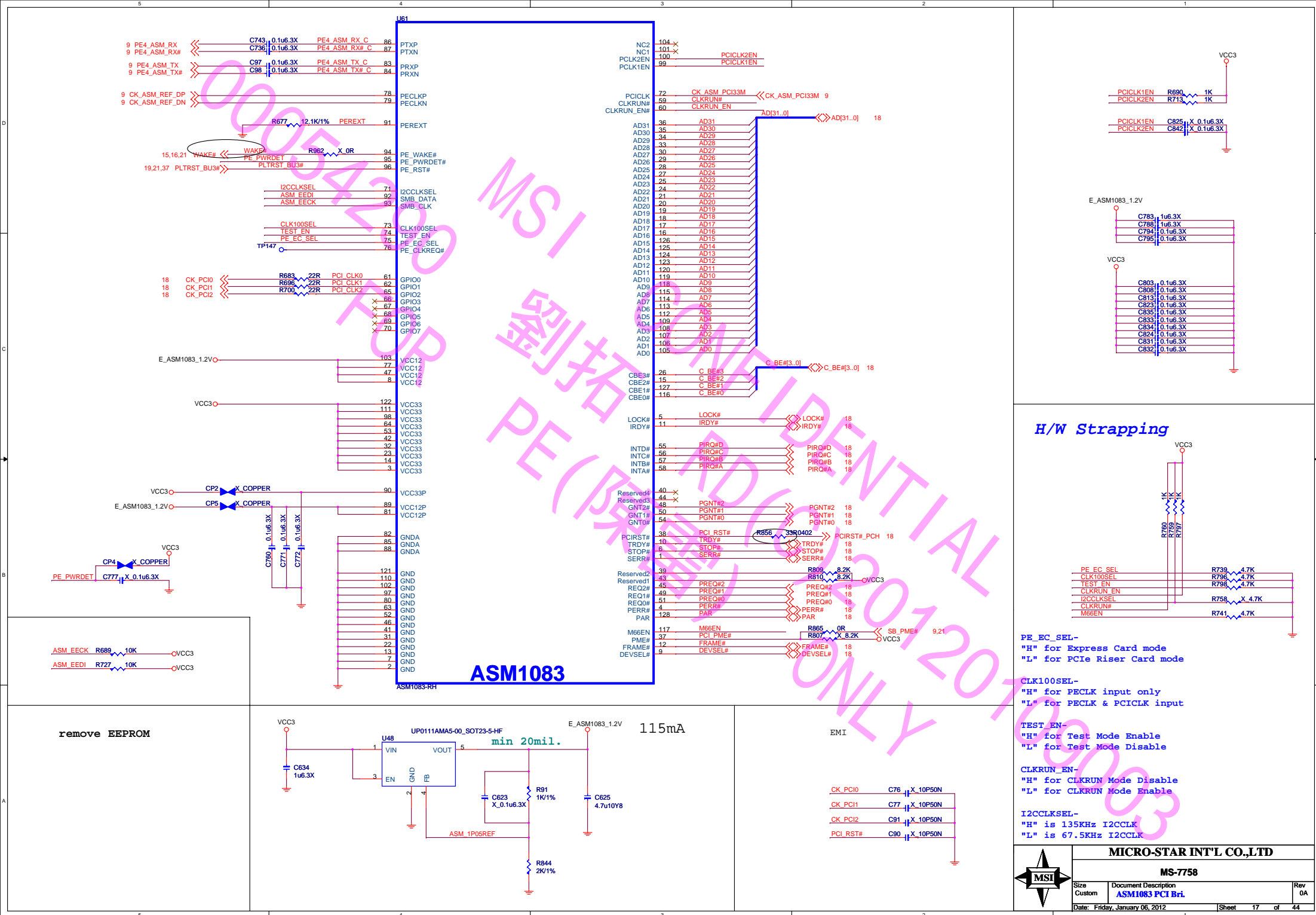
7,11,16,30,37,39 SMBCLK  
7,11,16,30,37,39 SMBDATA





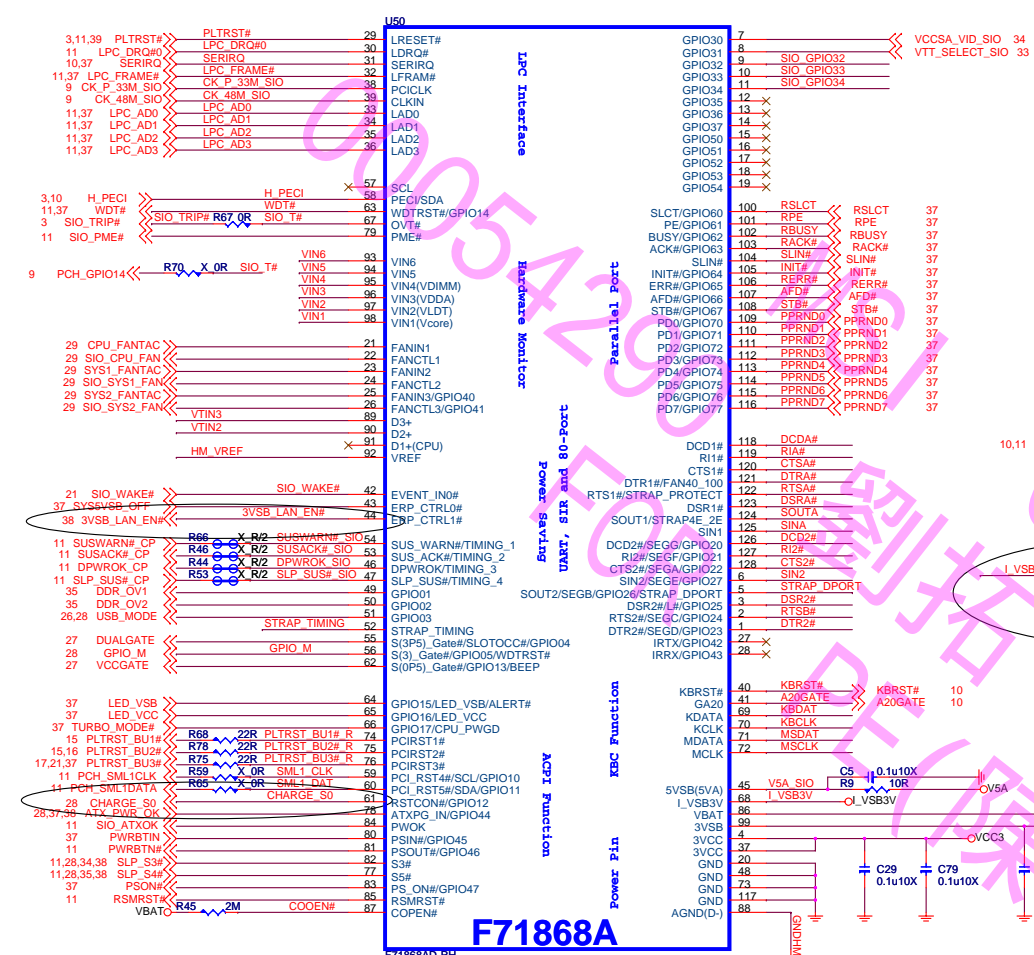
MS-7758

Size Custom	Document Description <b>PCIE3(X1) &amp; PCIE4(X4.) Slots</b>	Rev 0A
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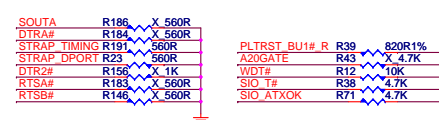




**LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor**

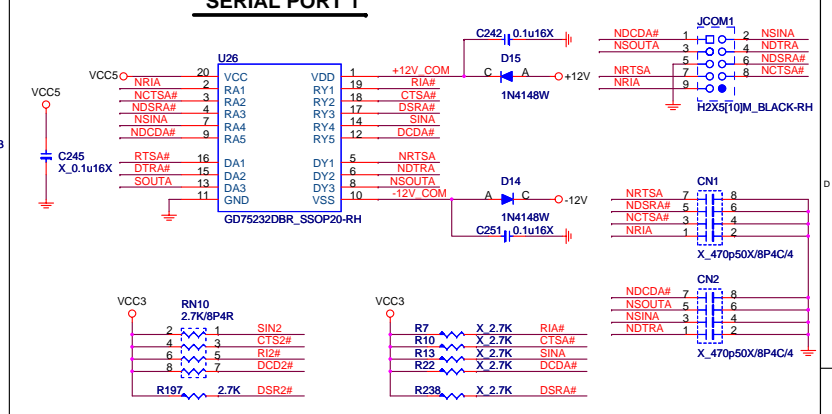
USB\_MODE, H\_PECI, SIO\_WAKE#, SIO\_TRIP#, SIO\_PME#, PCH\_GPIO14, CPU\_FANTAC, SIO\_CPU\_FAN, SYS1\_FANTAC, SIO\_SYS1\_FAN, SYS2\_FANTAC, SIO\_SYS2\_FAN, SIO\_WAKE#, SYS6\_VSB\_OFF, 3VSB\_LAN\_EN, SUSWARN#\_CP, SIO\_ACK#\_CP, DPWROK\_CP, SLP\_SUS#\_CP, DDR\_OV1, SLP\_SUS#\_CP, STRAP\_TIMING, DUALGATE, GPIO\_M, VCCGATE, LED\_VSB, LED\_VCC, TURBO\_MODE#, PLTRST\_BUI#, PLTRST\_BUI#, PLTRST\_BUI#, PLTRST\_BUI#, PCH\_SML1CLK, PCH\_SML1DATA, CHARGE\_S0, ATX\_PWR\_OK, SIO\_ATXOK, PWRBTN#, PWRBTN#, SLP\_S3#, SLP\_S4#, PSON#, RSMRST#, VBAT#

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP_TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP_DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
RTSA#		

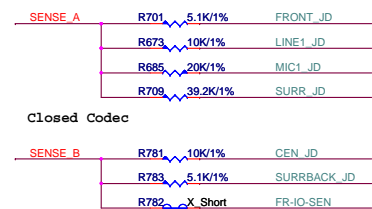
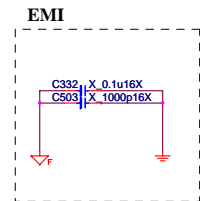


	GPIO34	GPIO33	GPIO32
H77	0	0	0
Z77	0	0	0
Z77_	0	0	1
USB CHARGE			

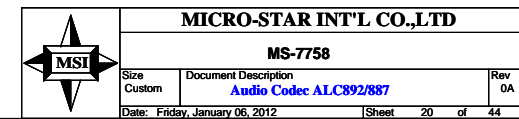
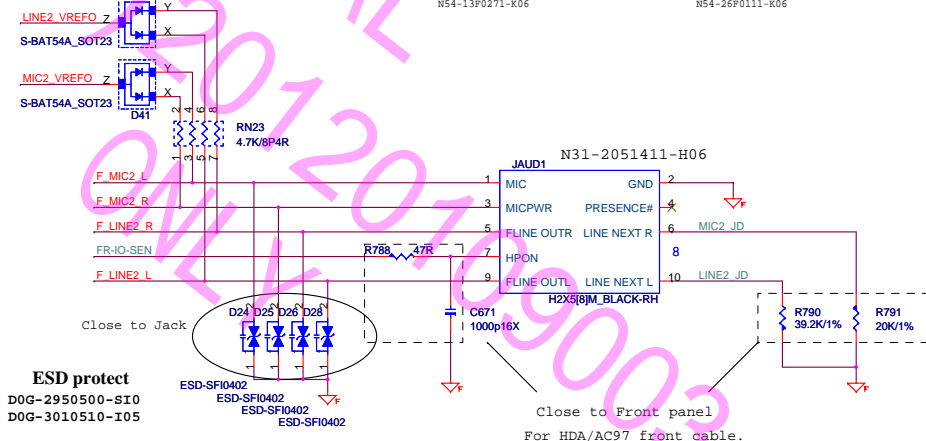
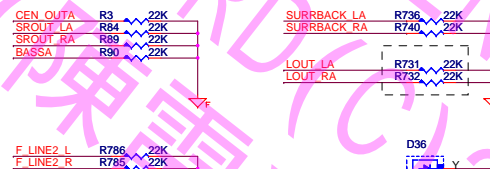
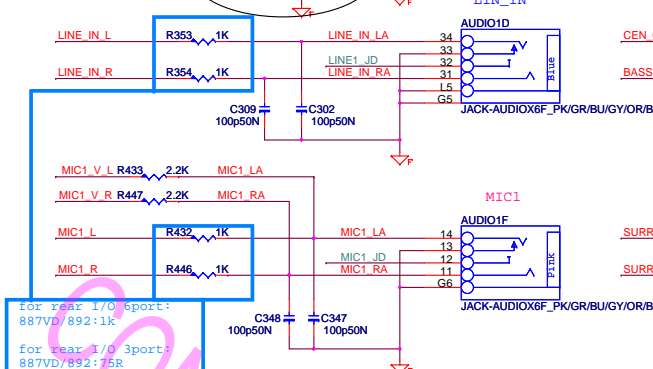
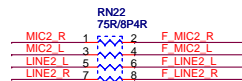
**OPT BOM**



## ALC892



## SPDIF OUT

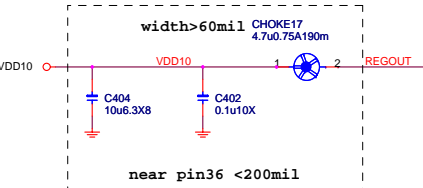
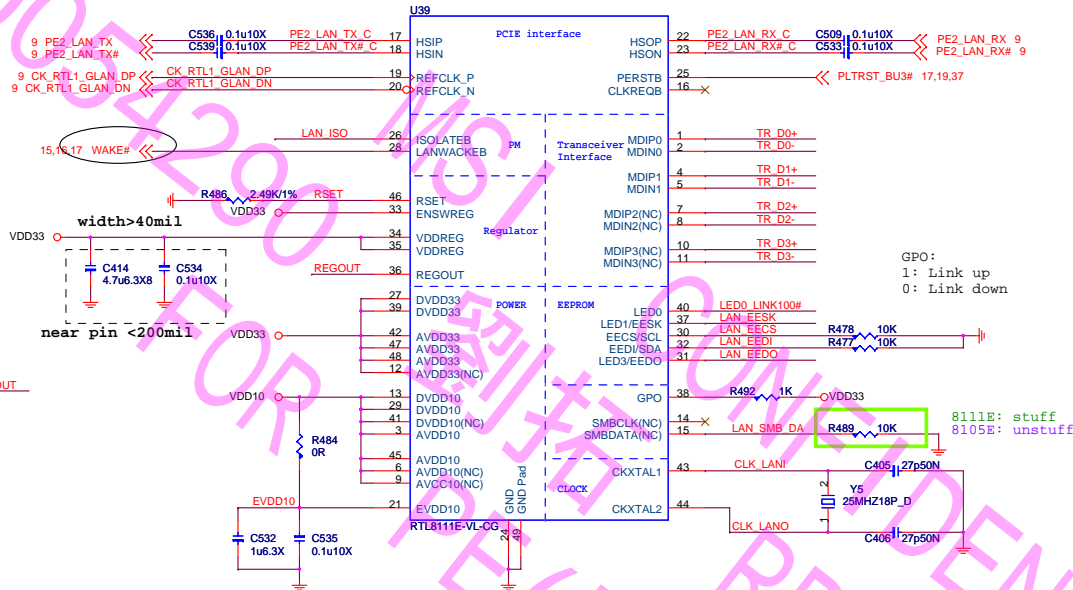


# RTL8111E Giga LAN

## RTL8105E 10/100M LAN

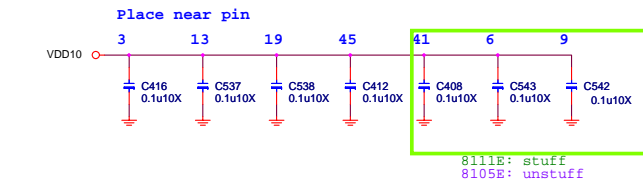
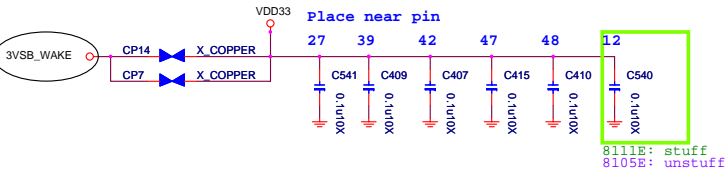


ENSWREG:  
1: Enable switching regulator  
0: Disable switching regulator



CHOKE(>0.6A) AVL:  
L04-47A7340-T04

3.3v Power on rise time : 1-100ms. MAX: 163mA



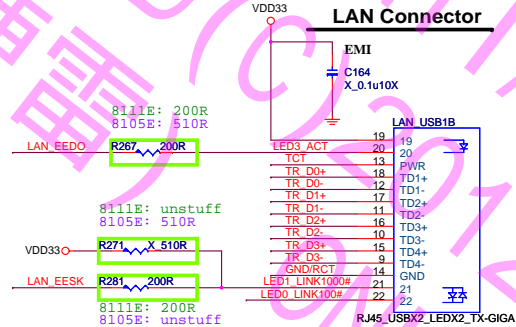
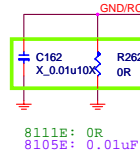
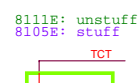
8111E POWER Consumption

	3.3v	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

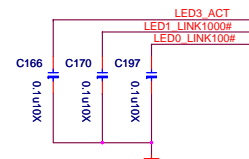
8105E POWER Consumption

	3.3v	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

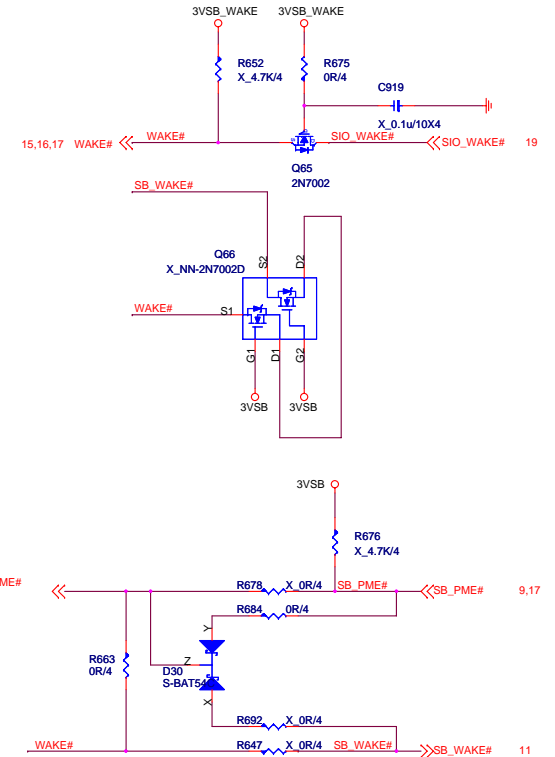
Pin49: 9 via from top layer to GND layer and make the via at the center of IC.



only support LED0+LED1/LED1+LED3 dual color LED combinations when using EEPROM



## LAN/PCIE/PCI Wake Up CTRL Circuit

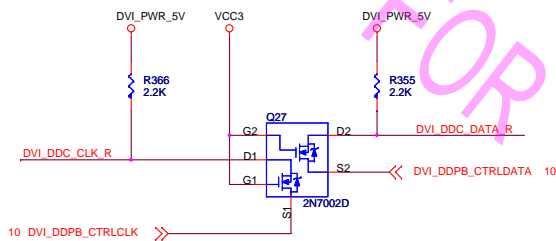


Giga-Lan	10/100-Lan
<b>N58-22F0731</b>	<b>N58-22F0771</b>
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	100 Green
100 Green	10 None
10 None	None
19	19
20	20
21	21
22	22

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

10 DVI\_DDPB\_CLK\_N << DVI\_DDPB\_CLK\_N C337 0.1u10X DVI\_C\_CLK\_N R498 680R DVI\_DATA\_CLK\_DN  
10 DVI\_DDPB\_CLK\_P << DVI\_DDPB\_CLK\_P C336 0.1u10X DVI\_C\_CLK\_P R524 680R DVI\_DATA\_CLK\_DP  
10 DVI\_DDPB\_TXN0 << DVI\_DDPB\_TXN0 C362 0.1u10X DVI\_C\_DATA0\_N R493 680R DVI\_DATA0\_DN  
10 DVI\_DDPB\_TXP0 << DVI\_DDPB\_TXP0 C361 0.1u10X DVI\_C\_DATA0\_P R507 680R DVI\_DATA0\_DP  
10 DVI\_DDPB\_TXN1 << DVI\_DDPB\_TXN1 C338 0.1u10X DVI\_C\_DATA1\_N R519 680R DVI\_DATA1\_DN  
10 DVI\_DDPB\_TXP1 << DVI\_DDPB\_TXP1 C339 0.1u10X DVI\_C\_DATA1\_P R523 680R DVI\_DATA1\_DP  
10 DVI\_DDPB\_TXN2 << DVI\_DDPB\_TXN2 C364 0.1u10X DVI\_C\_DATA2\_N R526 680R DVI\_DATA2\_DN  
10 DVI\_DDPB\_TXP2 << DVI\_DDPB\_TXP2 C363 0.1u10X DVI\_C\_DATA2\_P R514 680R DVI\_DATA2\_DP

C353 3.9950N  
C340 3.9950N  
C341 3.9950N  
C342 3.9950N  
C343 3.9950N  
C344 3.9950N  
C345 3.9950N  
C346 3.9950N  
C347 3.9950N  
C348 3.9950N  
C349 3.9950N



For EMI

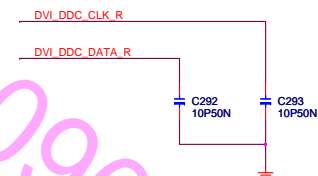
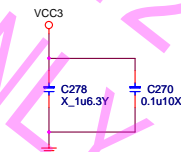
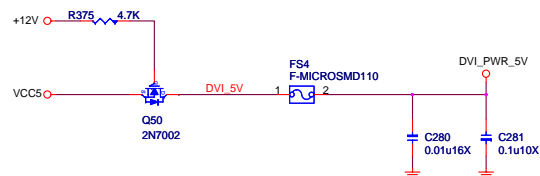
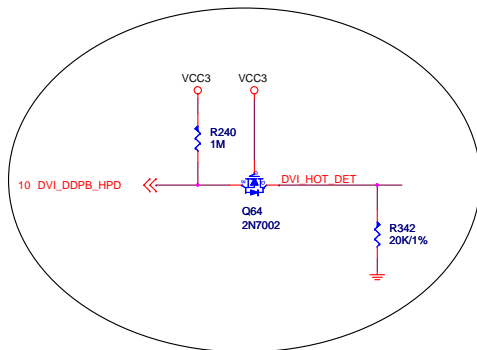
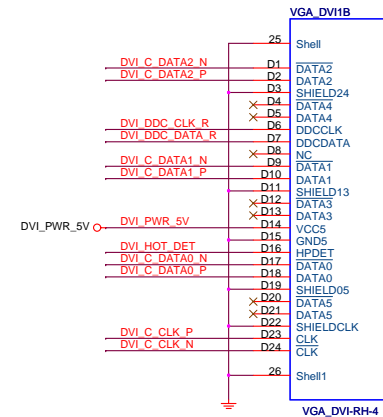
DVI\_C\_DATA0\_N  
DVI\_C\_DATA0\_P  
DVI\_C\_DATA1\_N  
DVI\_C\_DATA1\_P  
DVI\_C\_CLK\_N  
DVI\_C\_CLK\_P  
DVI\_C\_DATA2\_N  
DVI\_C\_DATA2\_P

R871  
X\_243R/1%

R874  
X\_243R/1%

R873  
X\_243R/1%

R872  
X\_243R/1%



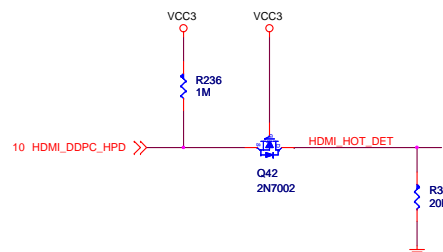
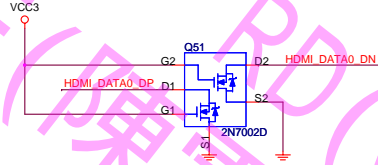
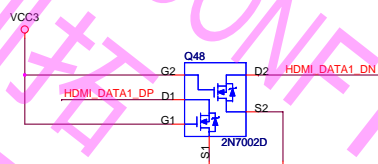
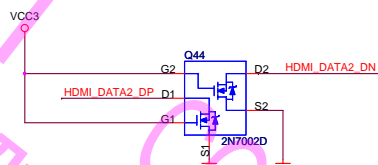
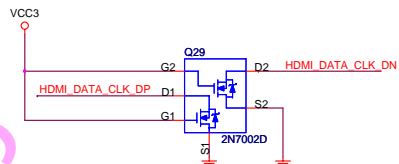
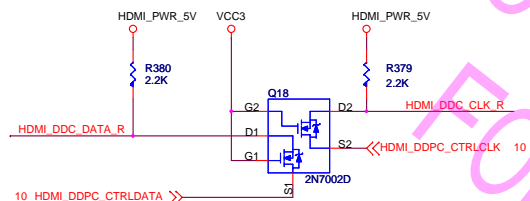
MICRO-STAR INT'L CO.,LTD

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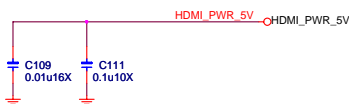
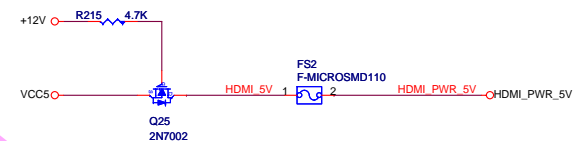
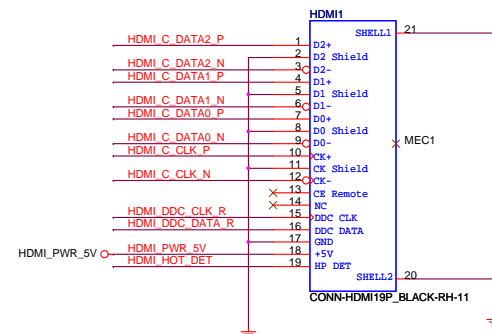
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

10 HDMI_DDPC_CLK_P	HDMI_DDPC_CLK_P	C140	0.1u10X	HDMI_C_CLK_P	R545	680R	HDMI_DATA_CLK_DP
10 HDMI_DDPC_CLK_N	HDMI_DDPC_CLK_N	C142	0.1u10X	HDMI_C_CLK_N	R553	680R	HDMI_DATA_CLK_DN
10 HDMI_DDPC_TX2_P	HDMI_DDPC_TX2_P	C134	0.1u10X	HDMI_C_DATA2_P	R527	680R	HDMI_DATA2_DP
10 HDMI_DDPC_TX2_N	HDMI_DDPC_TX2_N	C132	0.1u10X	HDMI_C_DATA2_N	R547	680R	HDMI_DATA2_DN
10 HDMI_DDPC_TX1_P	HDMI_DDPC_TX1_P	C136	0.1u10X	HDMI_C_DATA1_P	R548	680R	HDMI_DATA1_DP
10 HDMI_DDPC_TX1_N	HDMI_DDPC_TX1_N	C138	0.1u10X	HDMI_C_DATA1_N	R549	680R	HDMI_DATA1_DN
10 HDMI_DDPC_TX0_P	HDMI_DDPC_TX0_P	C124	0.1u10X	HDMI_C_DATA0_P	R552	680R	HDMI_DATA0_DP
10 HDMI_DDPC_TX0_N	HDMI_DDPC_TX0_N	C121	0.1u10X	HDMI_C_DATA0_N	R546	680R	HDMI_DATA0_DN



For EMI

HDMI_C_CLK_N	R235	X_180R/1%
HDMI_C_CLK_P	R235	X_180R/1%
HDMI_C_DATA0_N	R225	X_180R/1%
HDMI_C_DATA0_P	R225	X_180R/1%
HDMI_C_DATA1_N	R233	X_180R/1%
HDMI_C_DATA1_P	R233	X_180R/1%
HDMI_C_DATA2_N	R231	X_180R/1%
HDMI_C_DATA2_P	R231	X_180R/1%



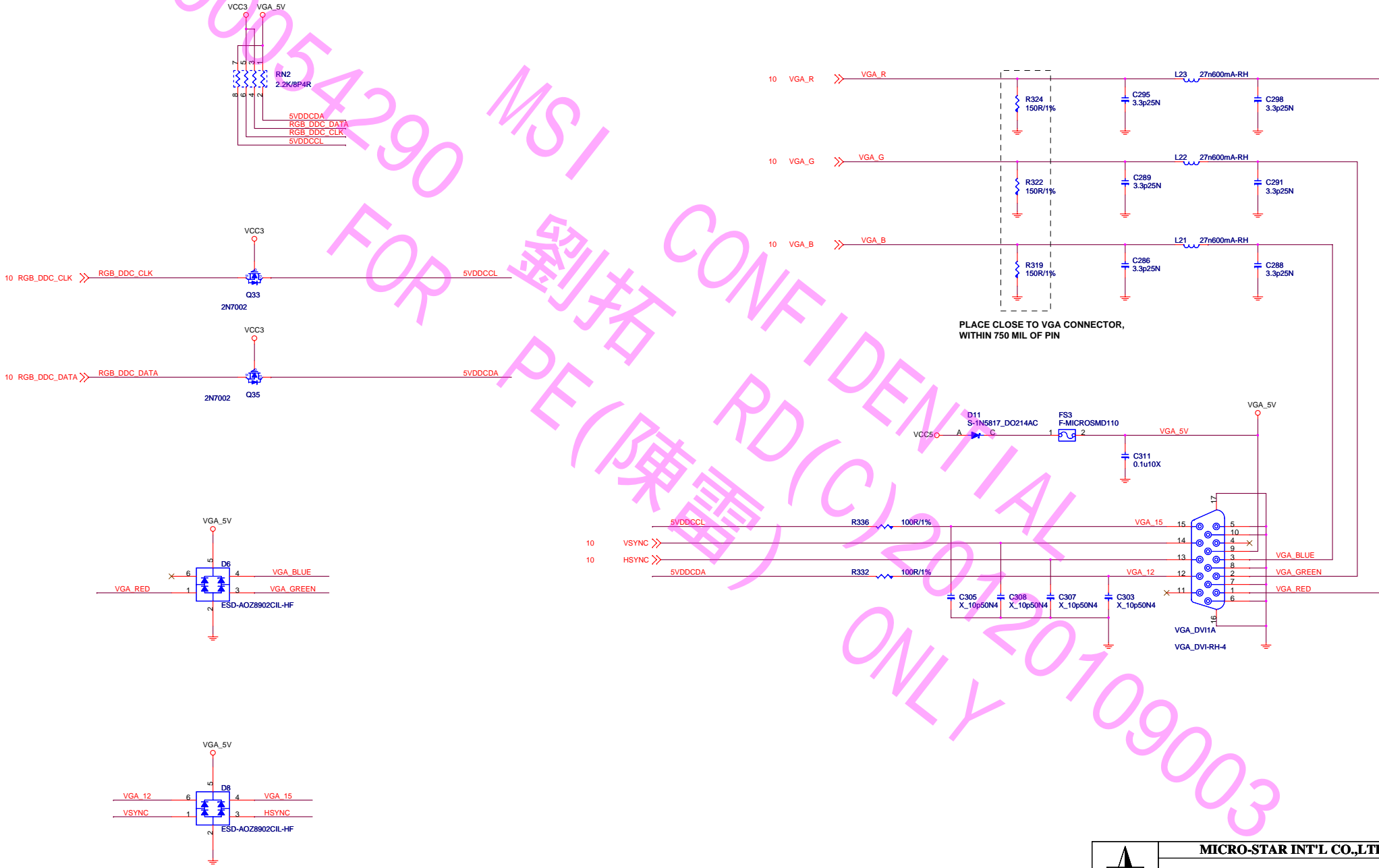
HDMI_DDC_CLK_R	C572	X_0.1u16X
HDMI_DDC_DATA_R	C571	X_0.1u16X
HDMI_HOT_DET	C570	X_0.1u16X



D-Sub

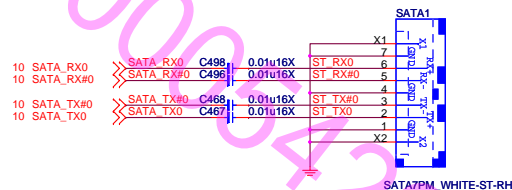
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

LevelShift

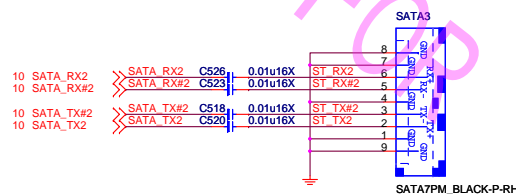


# SATA 6G PORT 0,1

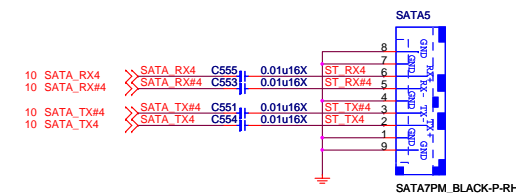
3.0 white



# SATA 3G PORT 2,3



# SATA 3G PORT 4,5



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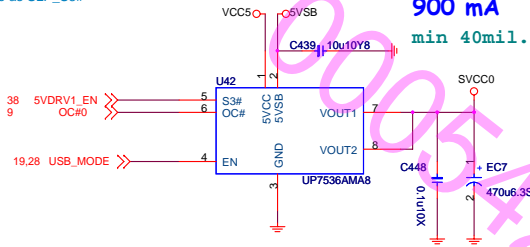
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# FRONT USB30 PORT 0,1

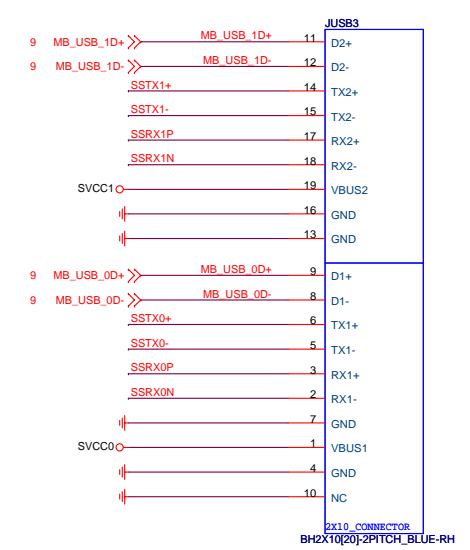
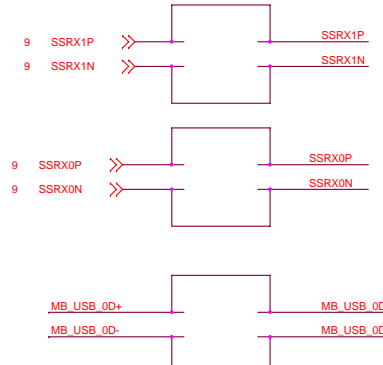
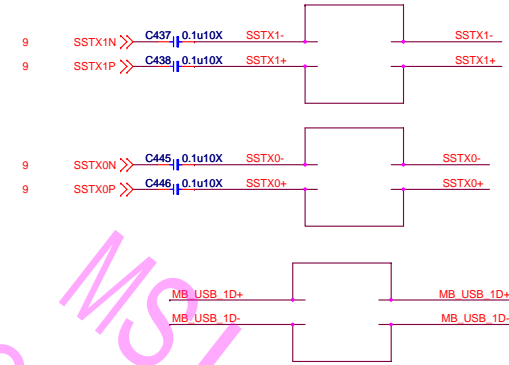
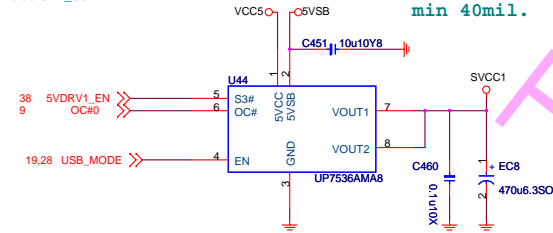
Same as SLP\_S3#

900 mA  
min 40mil.



Same as SLP\_S3#

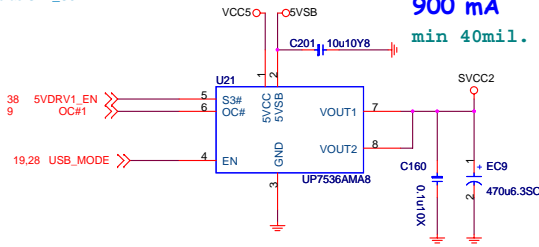
900 mA  
min 40mil.



# REAR USB30 PORT 2,3

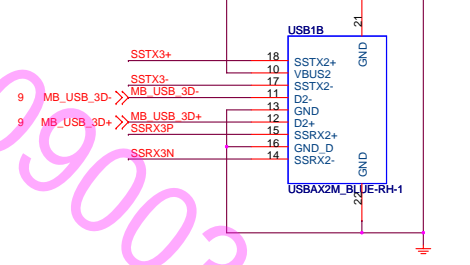
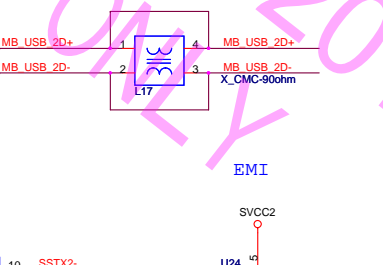
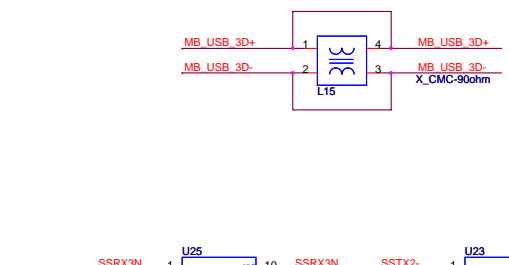
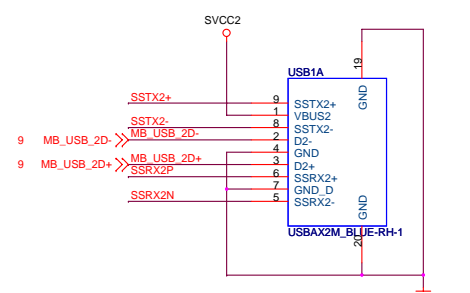
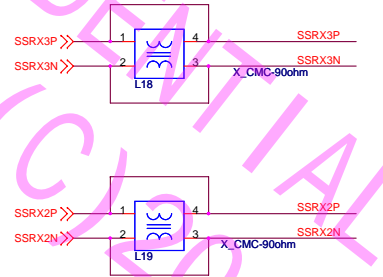
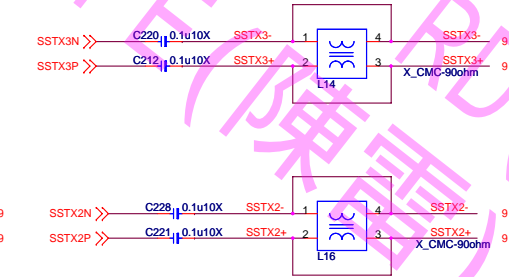
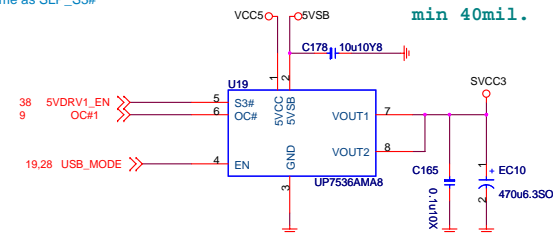
Same as SLP\_S3#

900 mA  
min 40mil.



Same as SLP\_S3#

900 mA  
min 40mil.



USB\_MODE  
Hi by BIOS programming,  
default h/w PD for avoid UP7536 Enable pin floating

USB_MODE States					
MODE	G3	S4/S5	S0	S3	
EUP Disable	0	0	1	1	
EUP Enable	0	0	1	1	



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USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	1	1	1
S0P5_Gate#	1	1	0

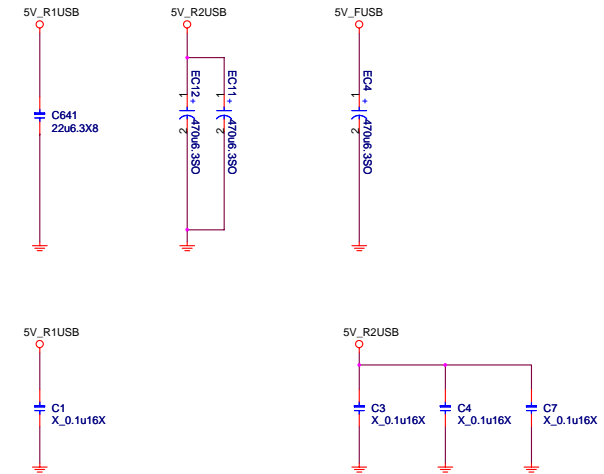
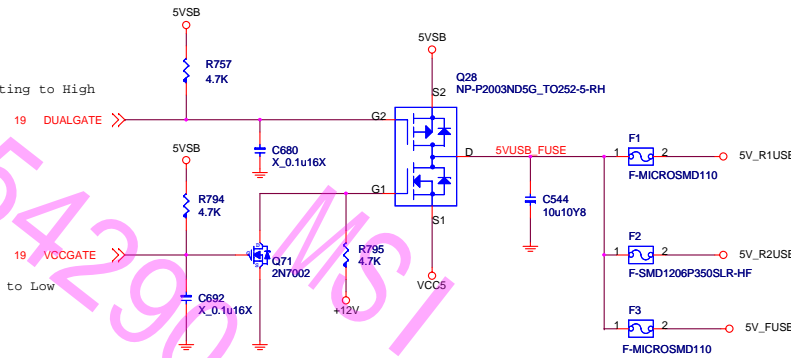
When PS2 in S5 not support wake , S3P5\_Gate# in S5 must setting to High

USB2.0/PS2 POWER Control			
MODE	S5	S0	S3
S3P5_Gate#	0	1	1
S0P5_Gate#	1	1	0

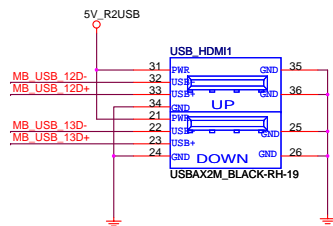
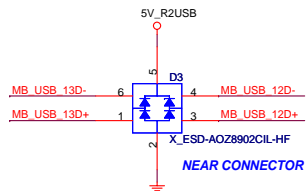
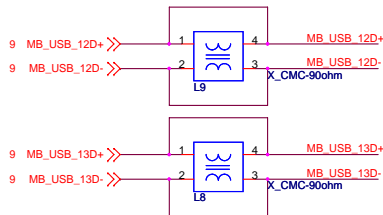
When PS2 in S5 support wake , S3P5\_Gate# in S5 must setting to Low

\*In S5# ( S3P5\_Gate # pin status is Tri-state, and can be programmed Low level.

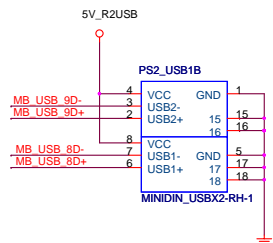
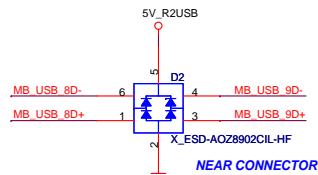
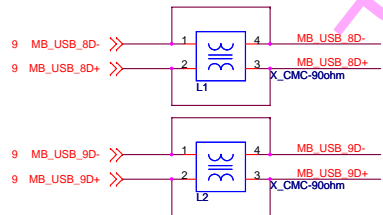
\*S3P5\_Gate# and S0P5\_Gate# can't setting to low together, avoid leakage voltage issue



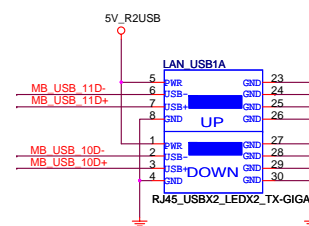
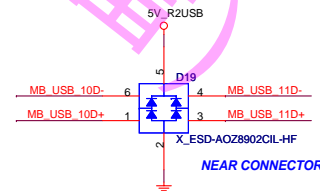
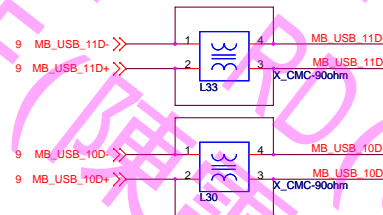
#### REAR USB PORT 12,13 (With LAN)



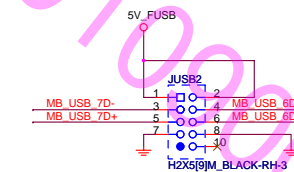
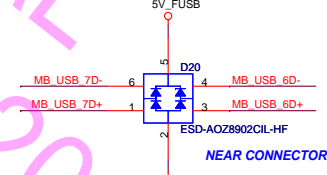
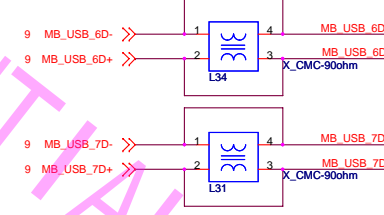
#### REAR USB PORT 8,9 (With HDMI)



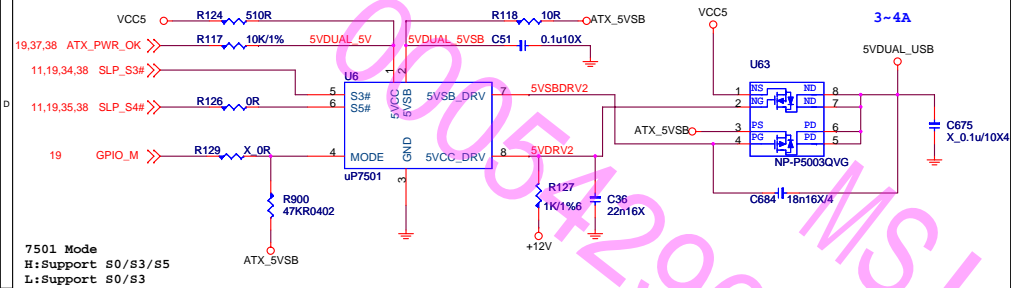
#### FRONT USB PORT 10,11(With PS2)



#### FRONT USB PORT 6,7



## 5VDUAL\_USB



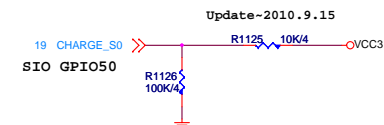
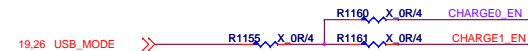
SIO GPIO40 Pin7 (I\_VSB3V)

USB\_CHARGE: (OD)

0: Don't support USB charge and resume.  
1: Support USB charge and resume.

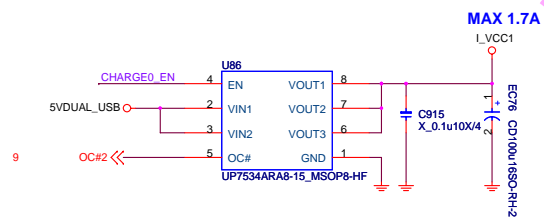
Power plug in , H/W default support USB charge.

Pin power I\_3VSB or VBAT  
Register power I\_3VSB or  
VBAT  
Register reset I\_3VSB or  
VBAT



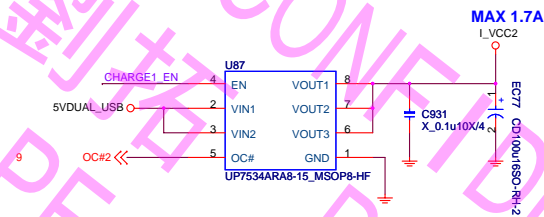
Update-2010.9.15

## USB POWER PORT 0 For USB Charging

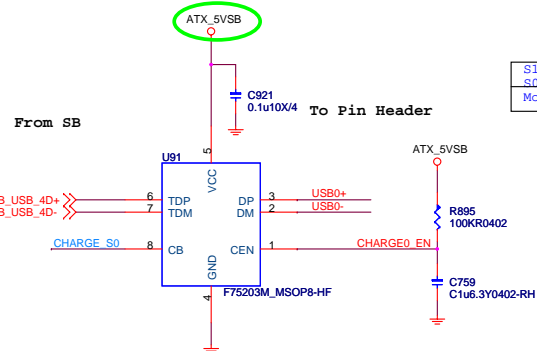
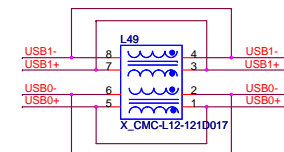


\*\* If your spec will not need bom option, please don't co-lay blue labels.

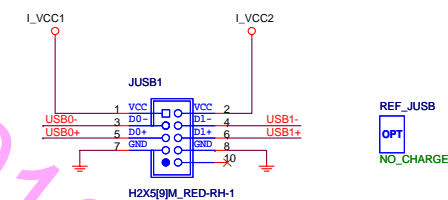
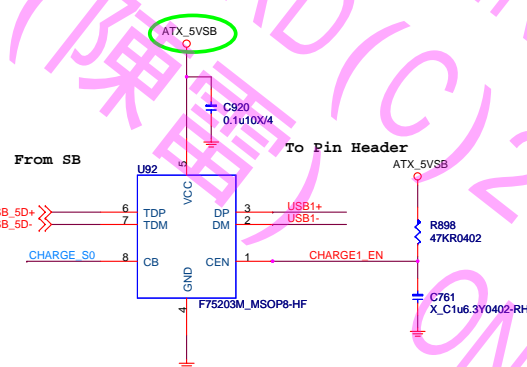
## USB POWER PORT 1 For USB Charging



## FRONT USB PORT 0,1

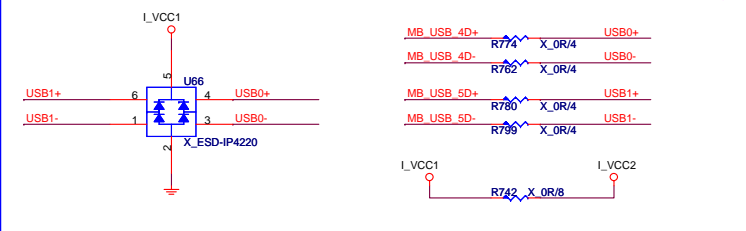


S1	0		0	1
S0	0		1	1
Mode	AUTO		A	Y



REF\_JUSB  
NO\_CHARGE

## COLAY remove USB charger ic



A type  
2.70V< D+ <3.1 V  
1.85V< D- < 2.1V  
For i-Pad / i-Phone 4G charges current up to 1.6A.

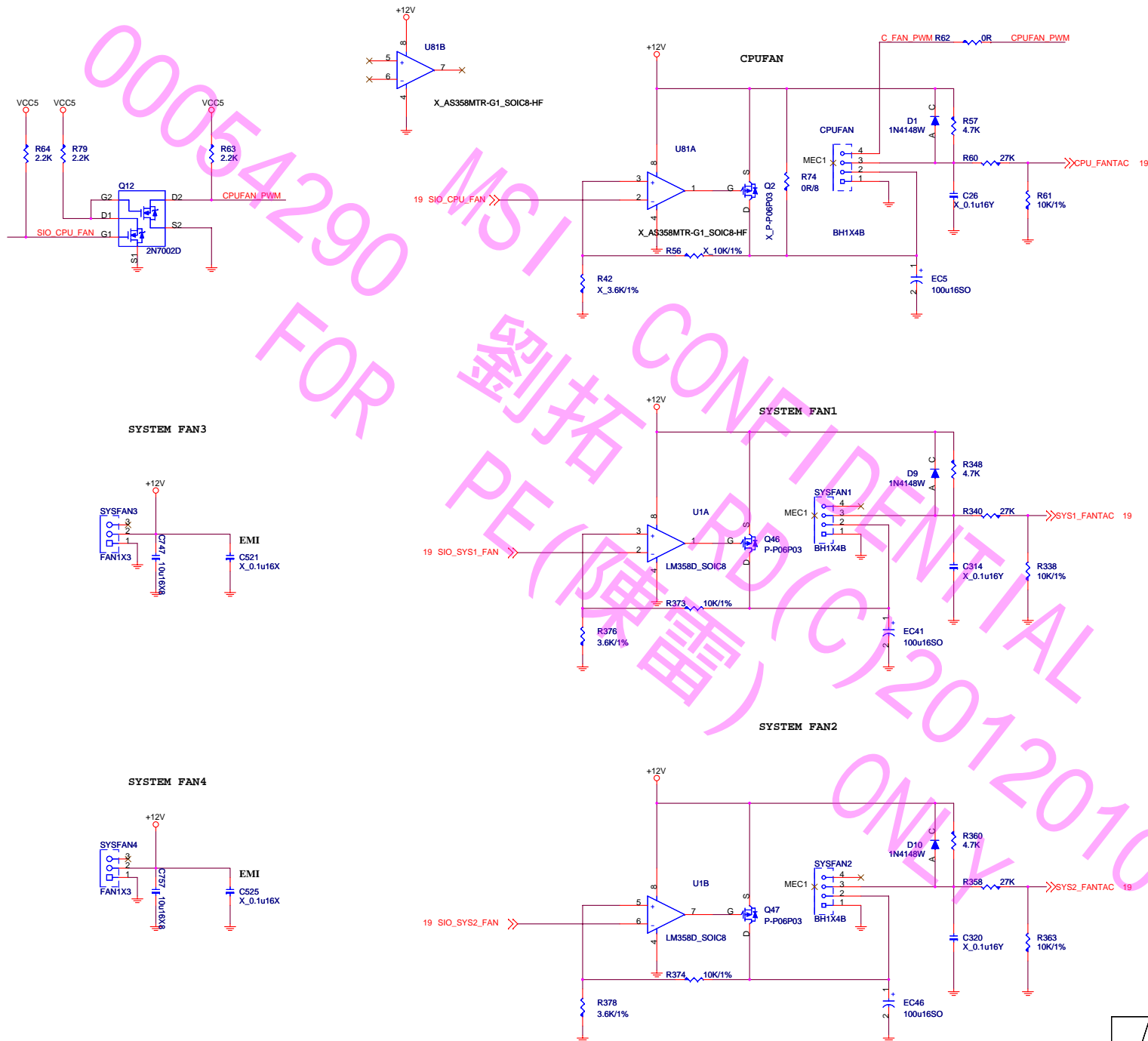
Please name the pin header JUSB1 and use SB USB0,1 link for charger port.

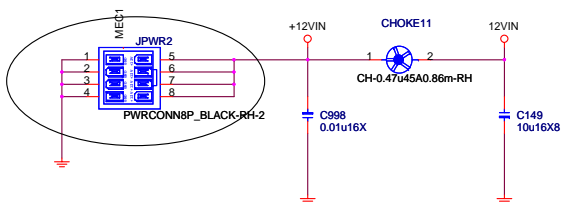
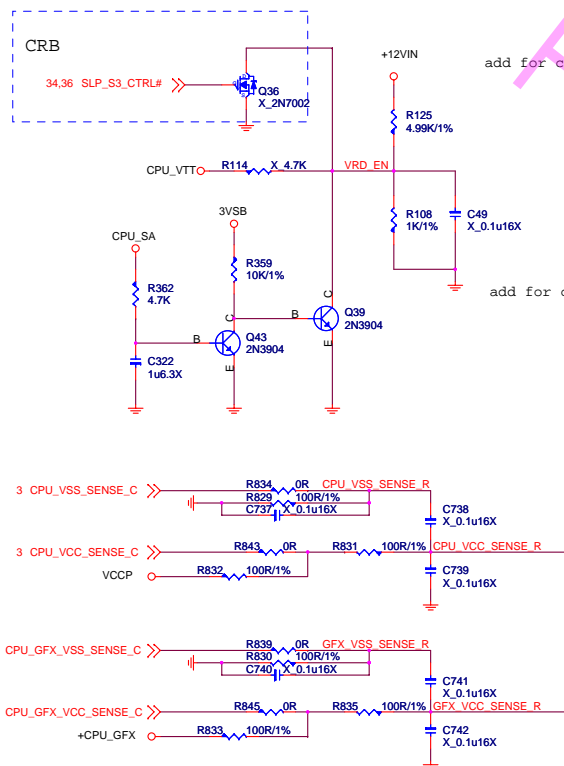
PI5USB14550 has internal EDS diode.

Title			USB FULL CHARGE
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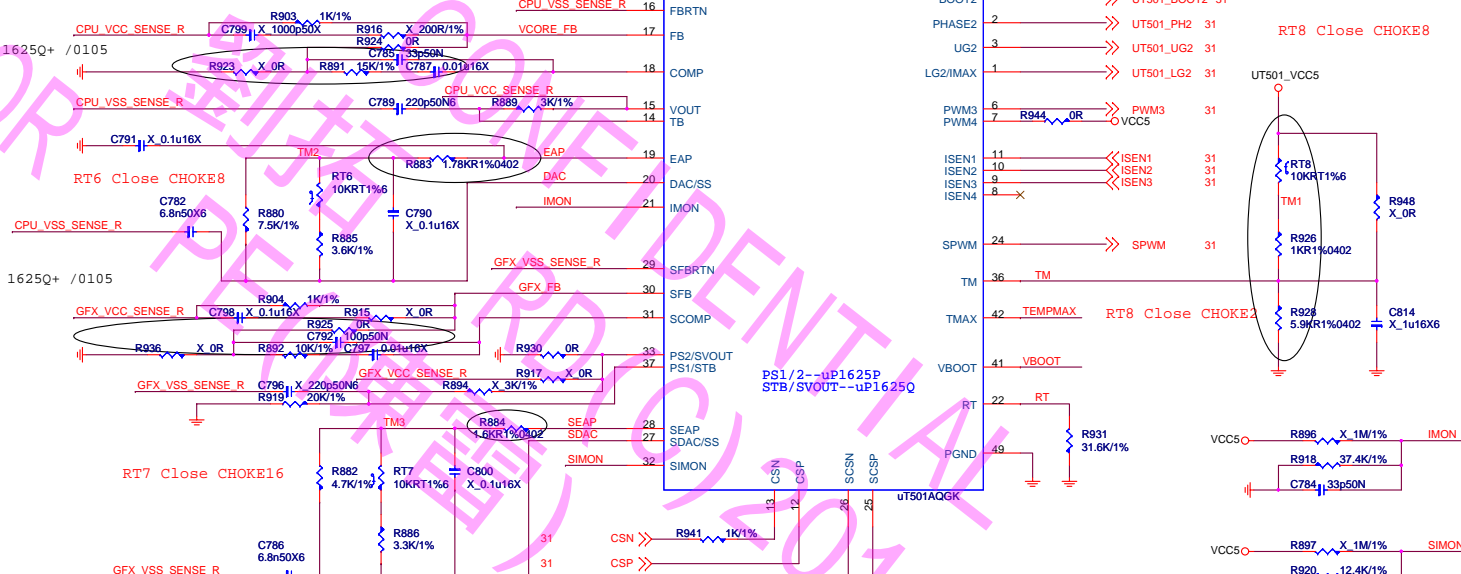
# FAN-COUNTROL CIRCUIT



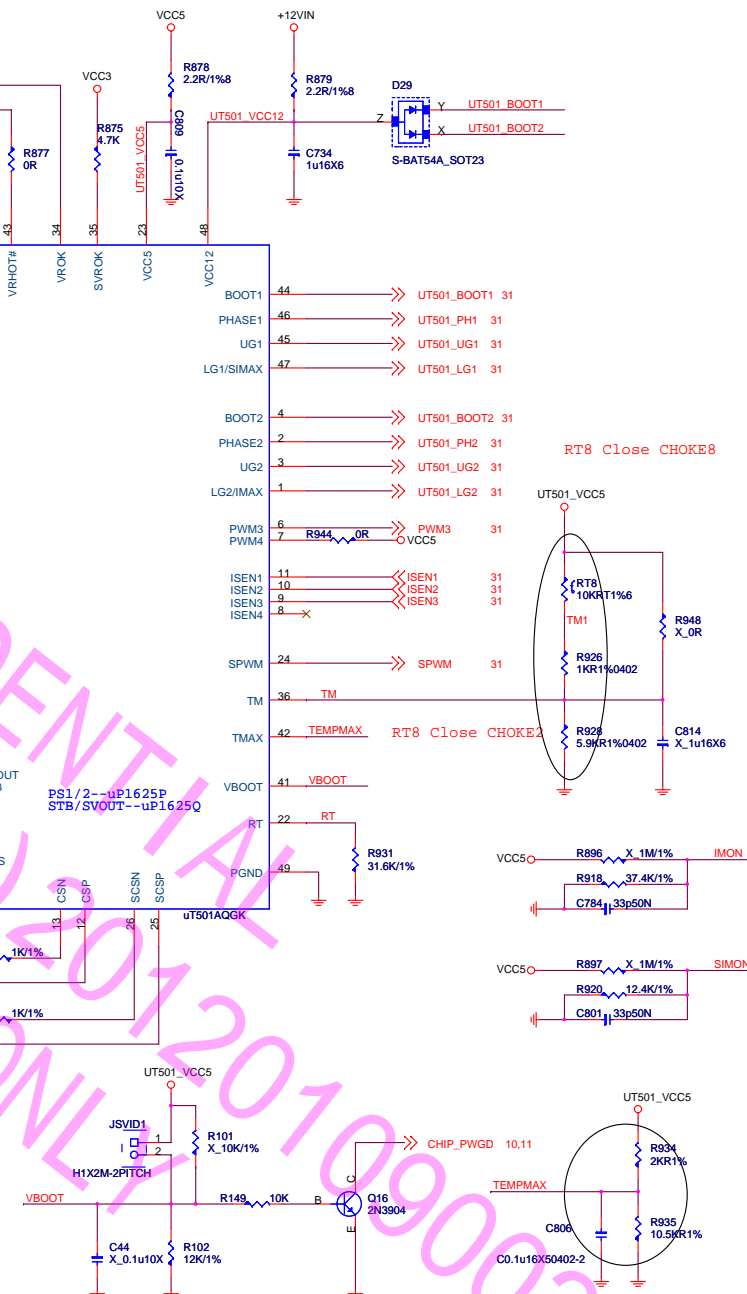
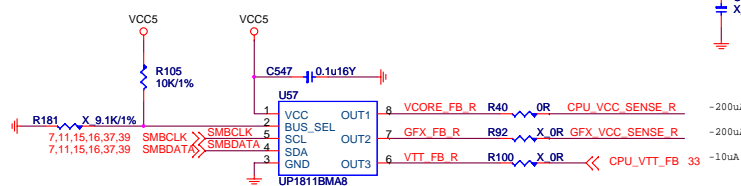


```
add for co_lay 16250+ /0105
```

```
add for co_lay 1625Q+ /0105
```

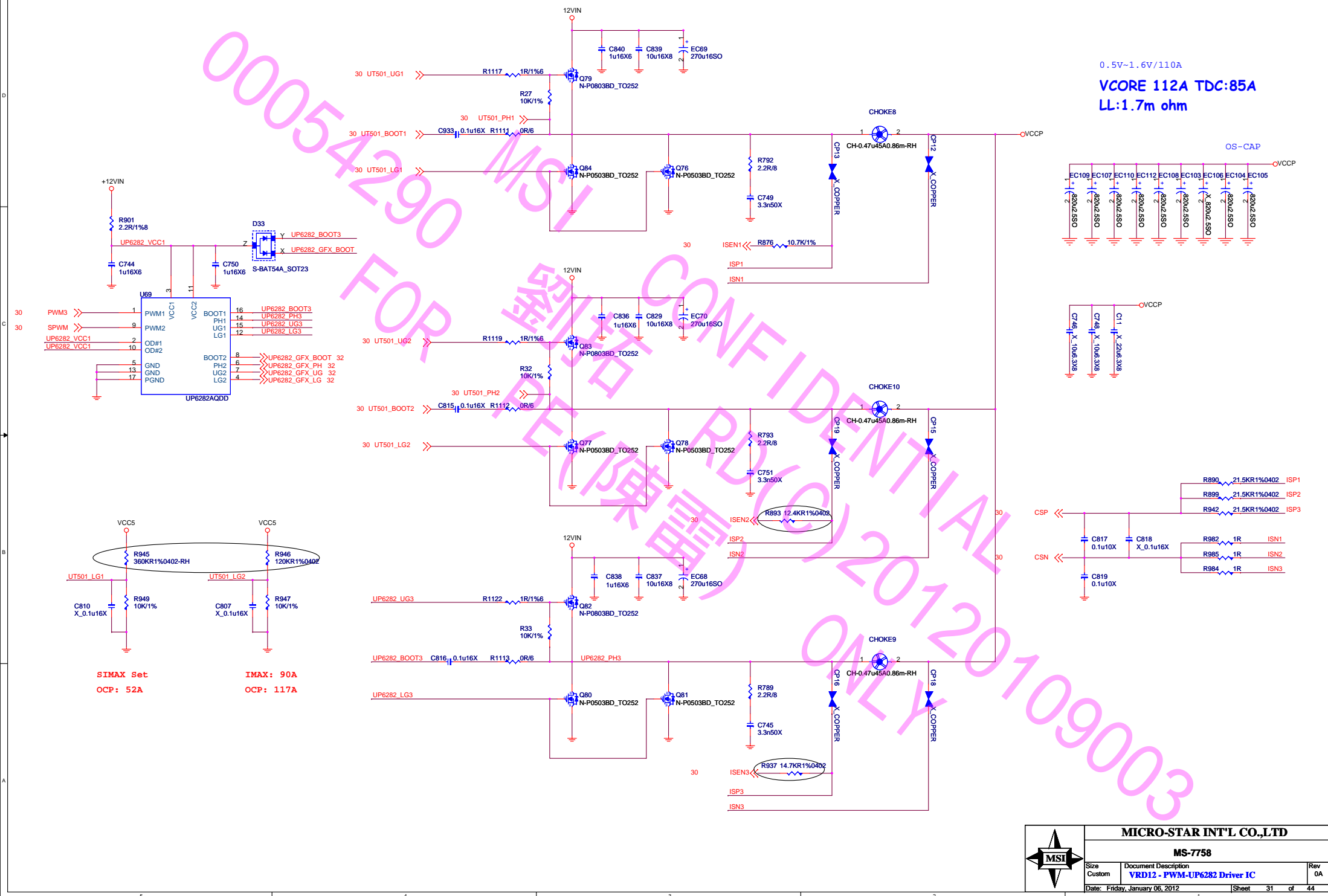


0x20: RH=10K, RL=OPEN						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

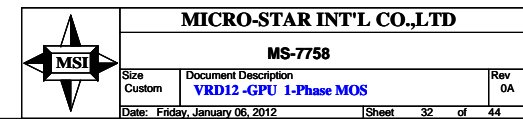


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**35A FOR CPU**

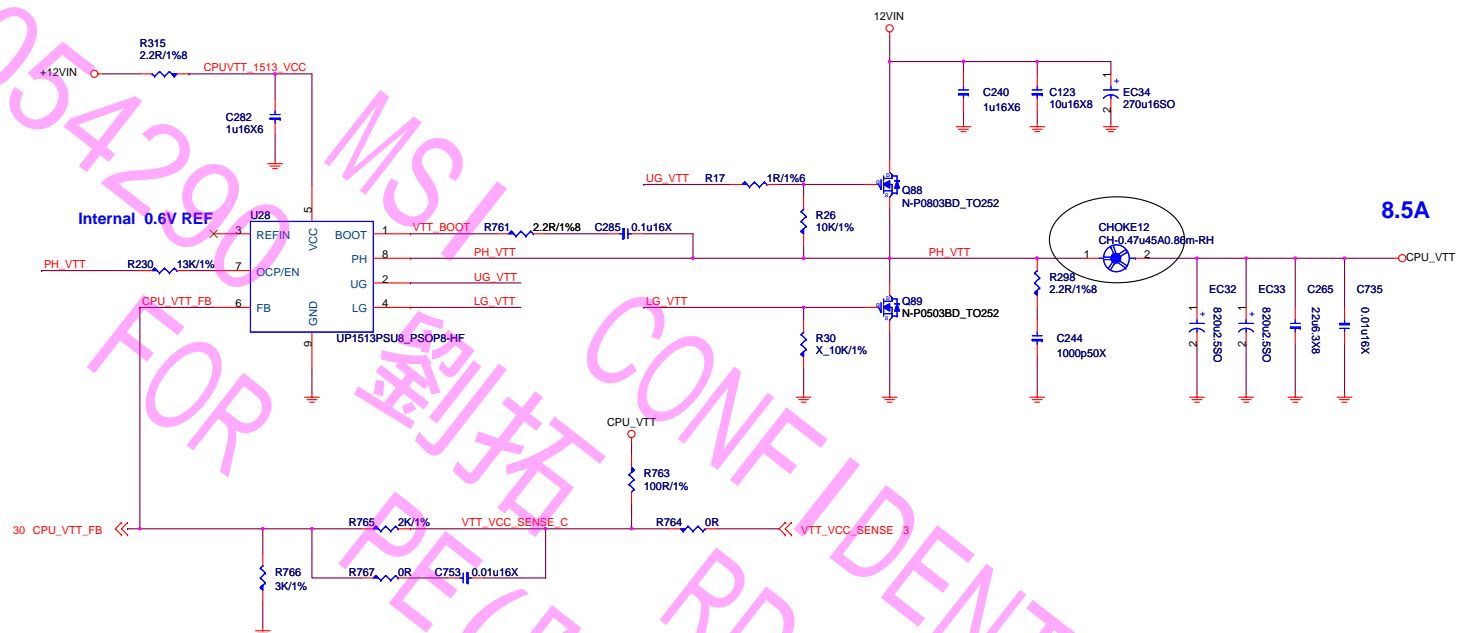


CPU\_VTT:1.05/1.00 MAX 17.3A

CPU VTT 8.5A SA Core =8.8A

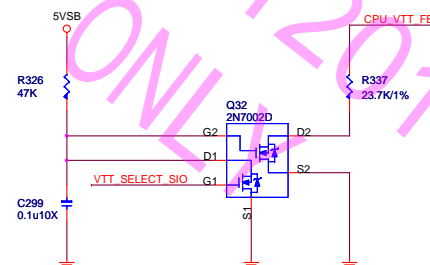
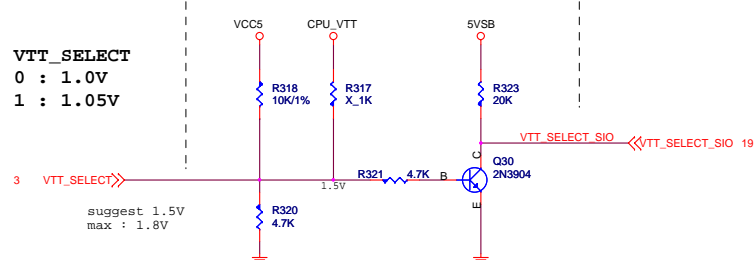
8.5A FOR CPU

$I_{\text{ripple}} = 1.92(\text{vtt}) + 1.88(\text{sa})$   
 $5 * 1 = 5\text{A} > 3.8\text{A}$



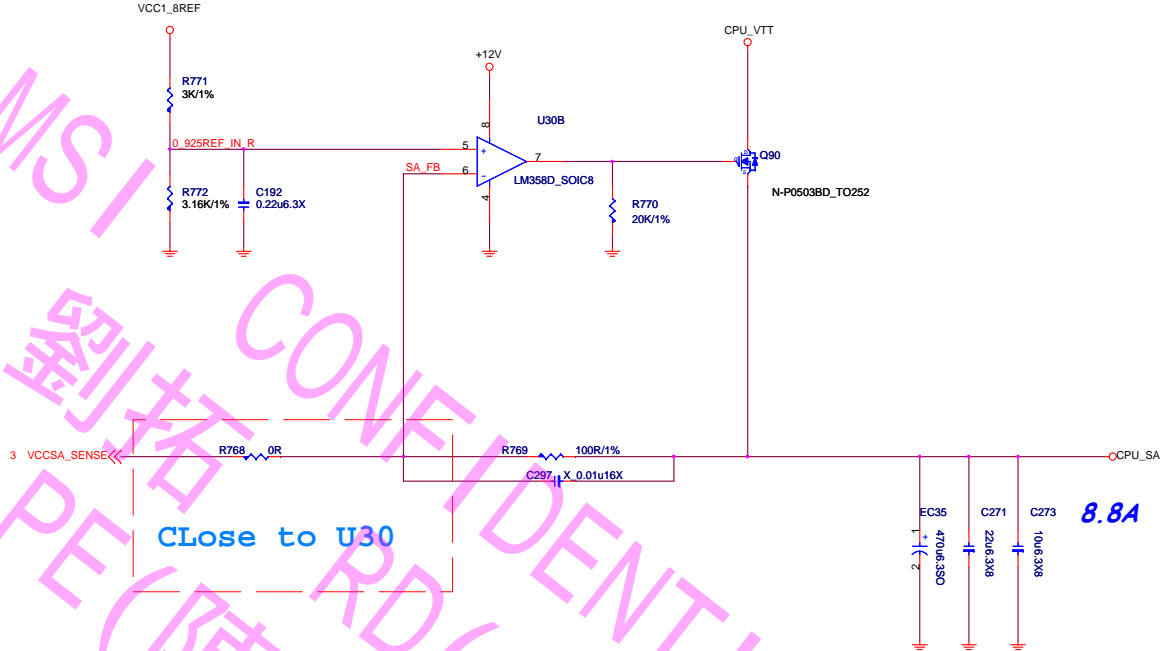
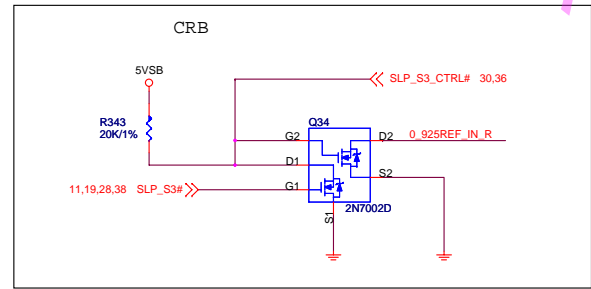
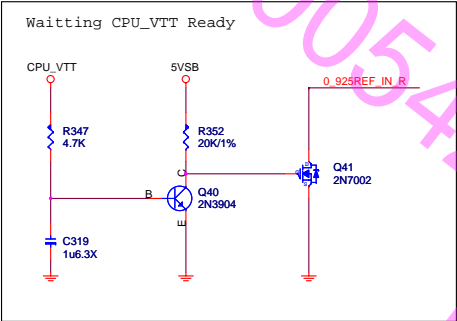
VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V



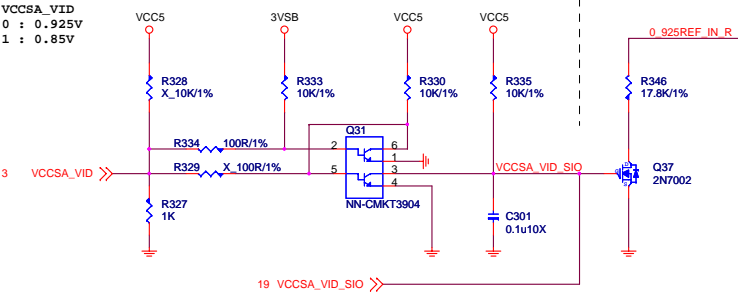
CPU\_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V





# DDR Power:1.5V

DDR3\_1.5V 4.75A+15A+1A=20.75A

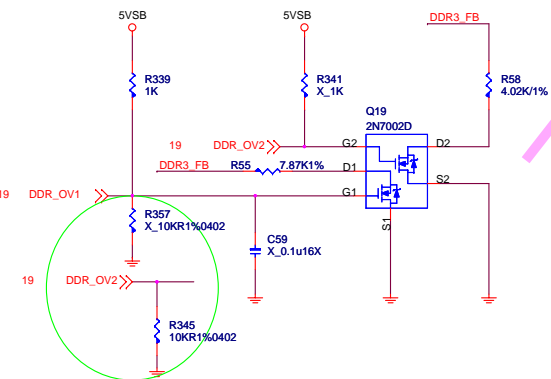
4.75A FOR CPU

15A FOR 4DIMM

1A FOR DDR VTT

Tripple=8A  
4.7\*2\*1=9.4A>8A

## DDR OV



\*Default 1.5V

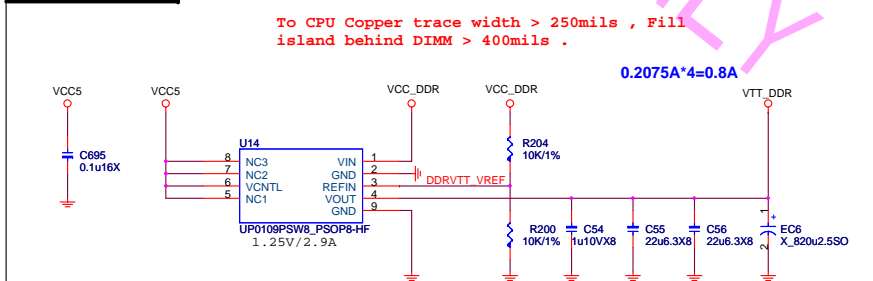
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR\_OV1 = GPIO01(S/IO)

DDR\_OV2 = GPIO02(S/IO)

$$((R221/R226)+1)*0.6=1.5V$$

## DDR VTT Power

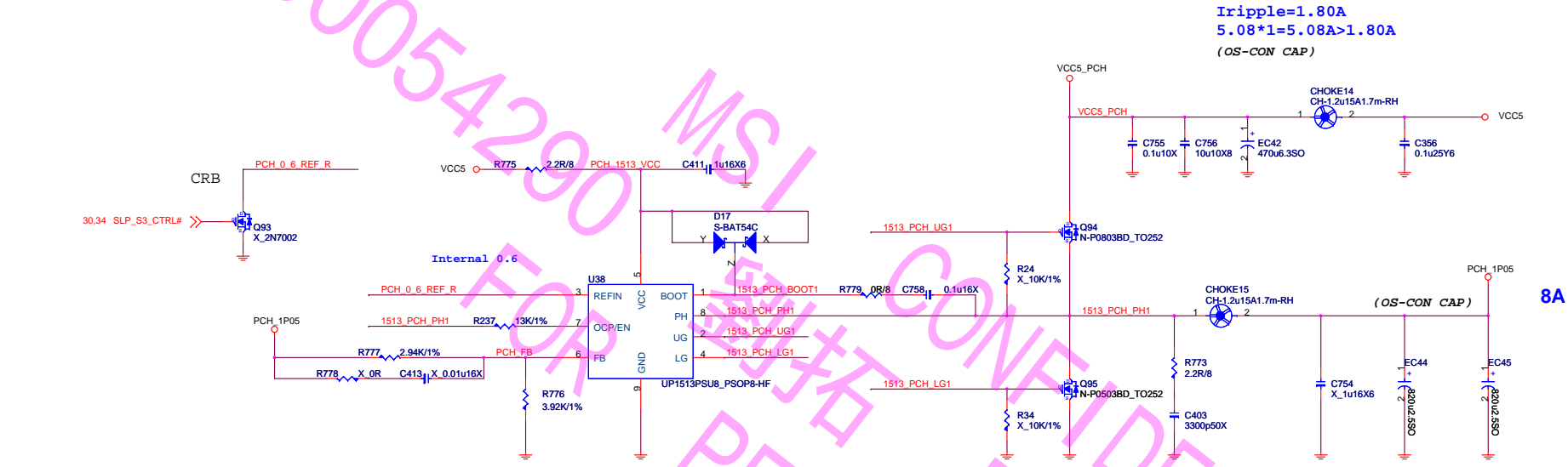


To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

$$0.2075A*4=0.8A$$

P.S. Only for meet Intel power down sequence.

PCH Power:1.05V  
PCH Core 6.2A+1.8A=8A  
6.2A FOR PCH  
1.8A FOR ME CORE

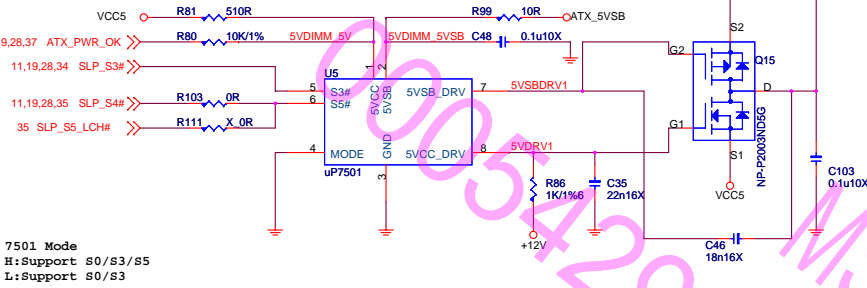


Tripple=1.80A  
5.08\*1=5.08A>1.80A  
(OS-CON CAP)

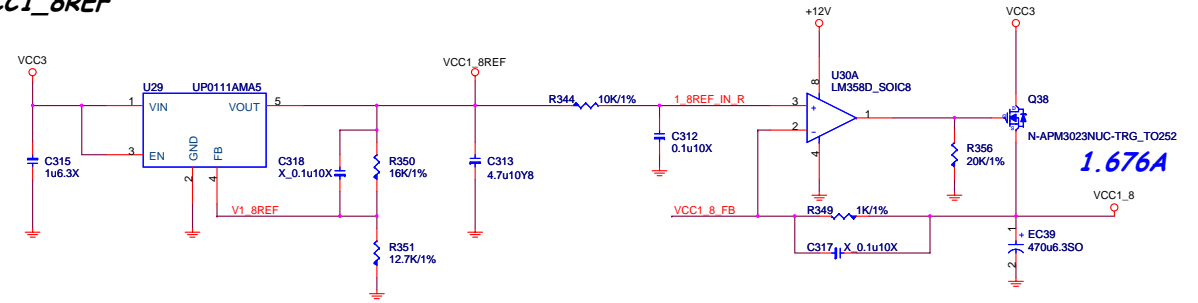
8A



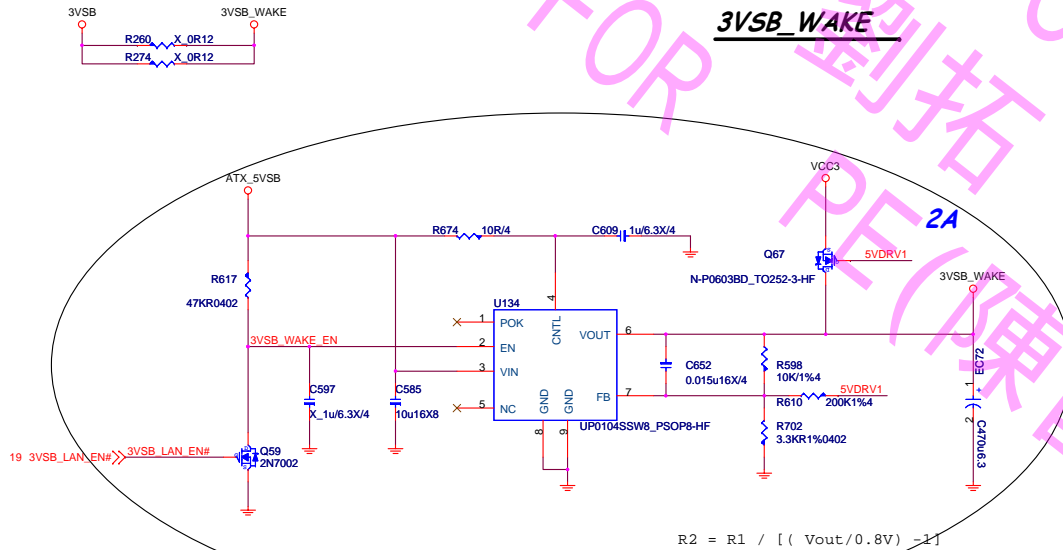
## 5VDIMM FOR DDR



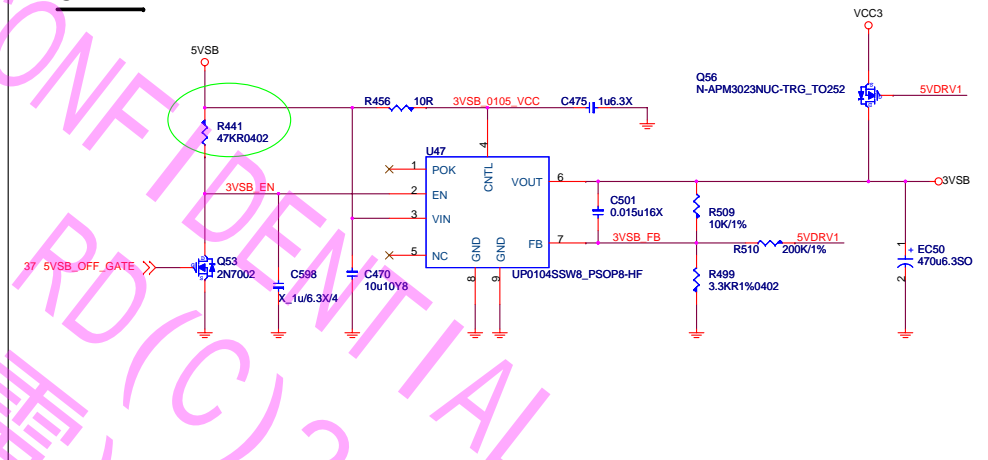
## VCC1\_8REF



## 3VSB\_WAKE

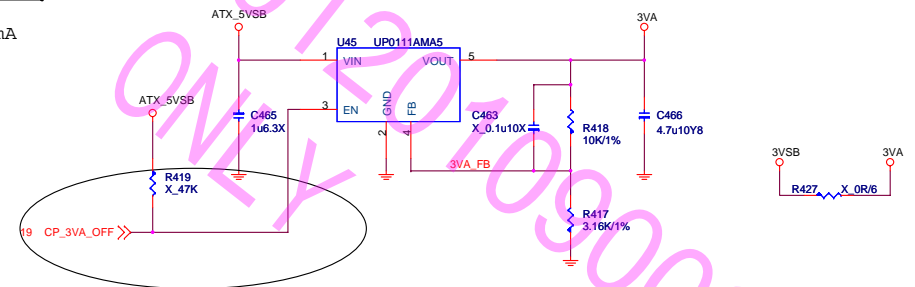


## 3VSB



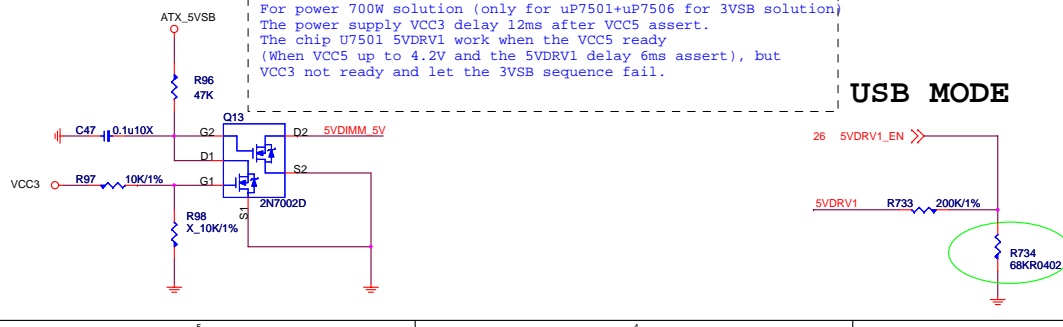
## 3VA

20mA



## USB MODE

For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.

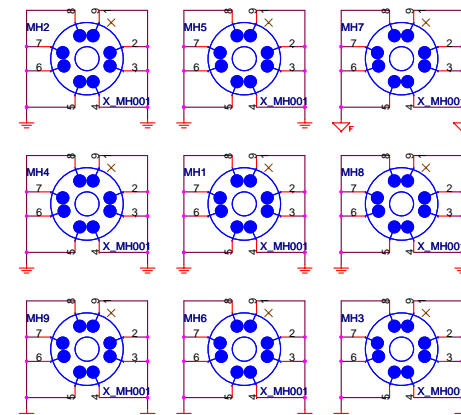


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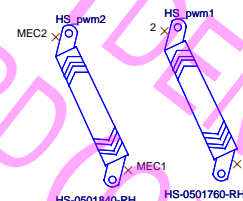
## Mounting Holes



### Voltage test point



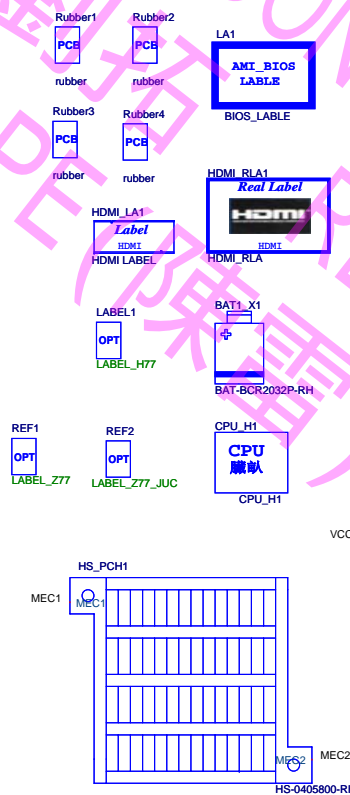
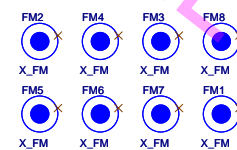
## HEATSINK



## Simulation

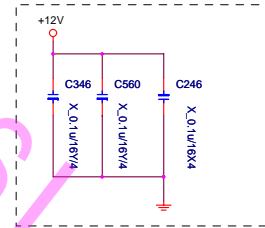
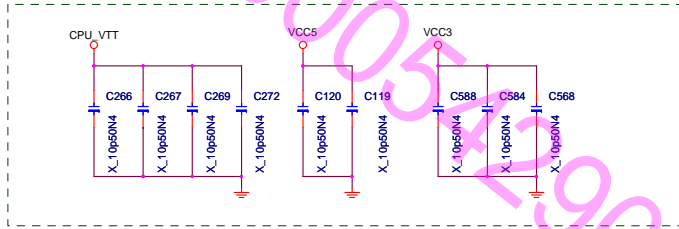


## Optical Fiducial Marks-120



EMI:cap. for signal return path

EMI



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